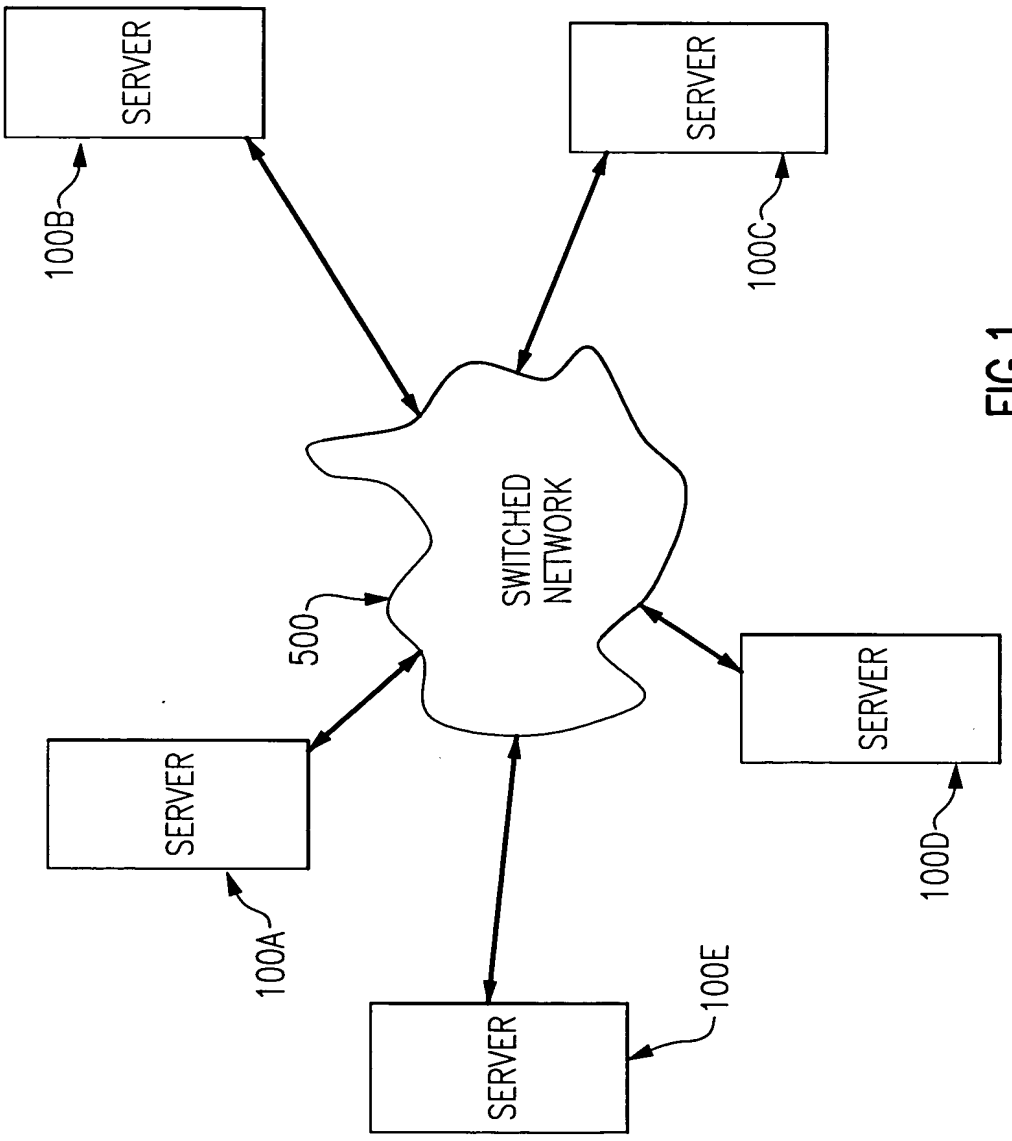

FIG.1

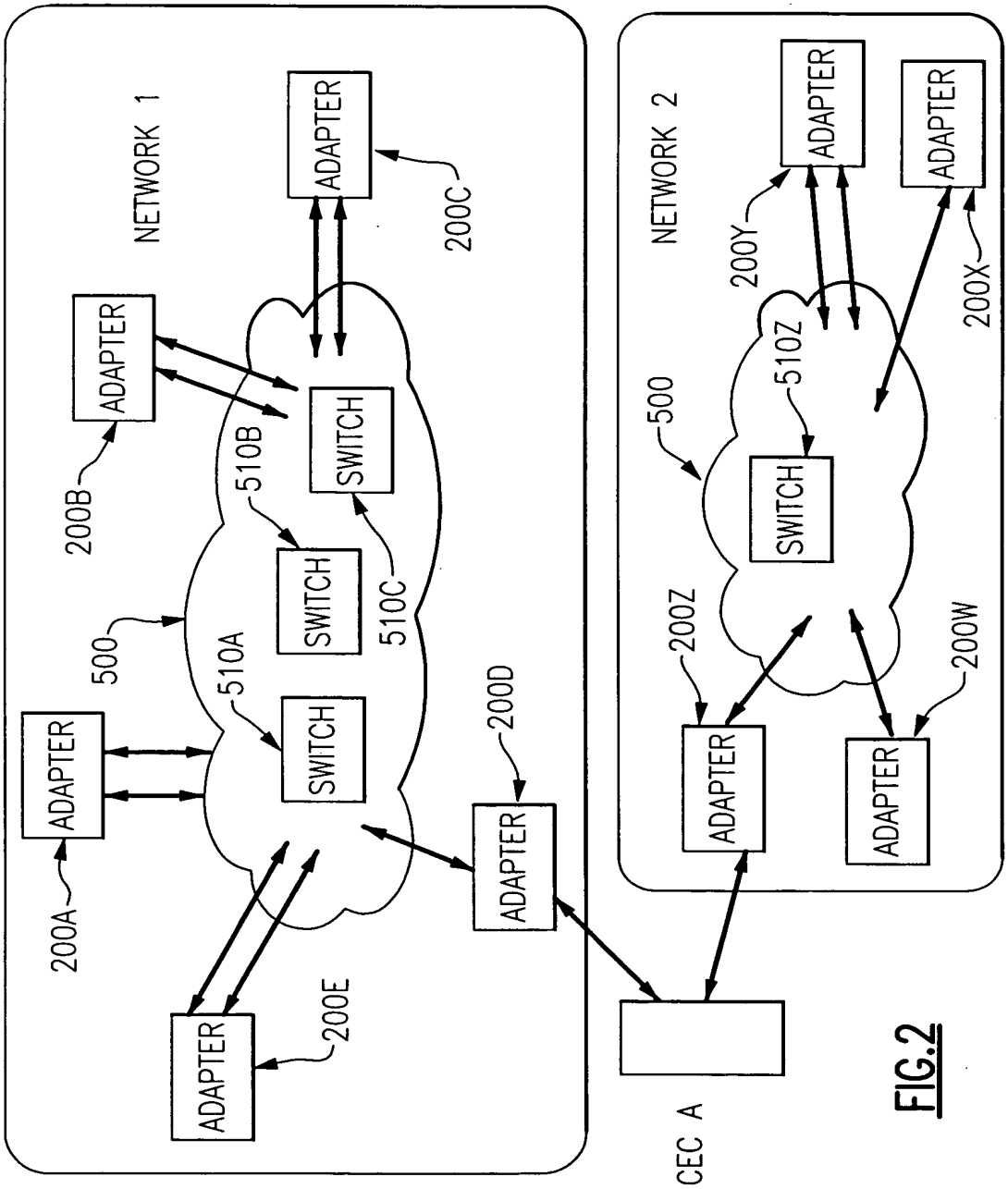
NETWORK 1
NETWORK 2
ADAPTER
SWITCH
200A
200B
200C
200D
200E
200W
200X
200Y
200Z
500
510A
510B
510C
510Z
CEC A

FIG.2

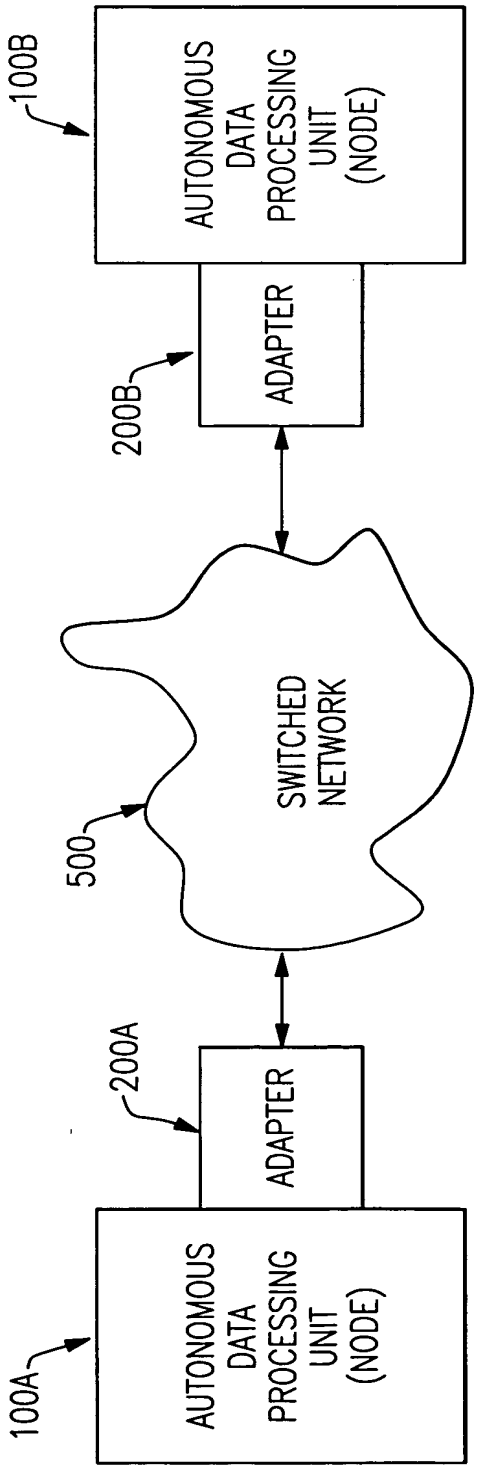
100B
AUTONOMOUS DATA PROCESSING UNIT (NODE)
200B
ADAPTER
500
SWITCHED NETWORK
200A
ADAPTER
100A
AUTONOMOUS DATA PROCESSING UNIT (NODE)

FIG.3

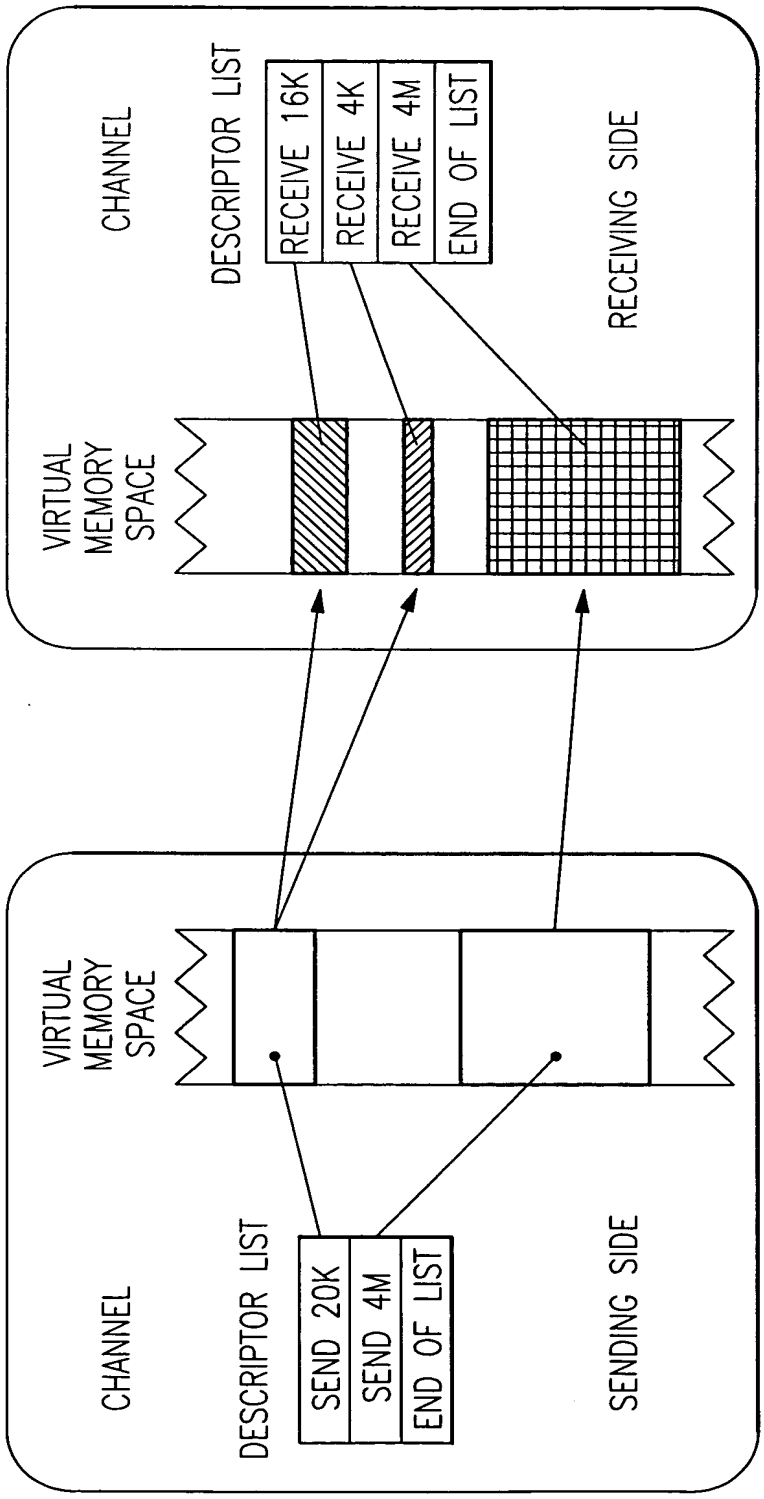
CHANNEL
DESCRIPTOR LIST
RECEIVE 16K
RECEIVE 4K
RECEIVE 4M
END OF LIST
RECEIVING SIDE
VIRTUAL MEMORY SPACE
VIRTUAL MEMORY SPACE
CHANNEL
DESCRIPTOR LIST
SEND 20K
SEND 4M
END OF LIST
SENDING SIDE

FIG.4

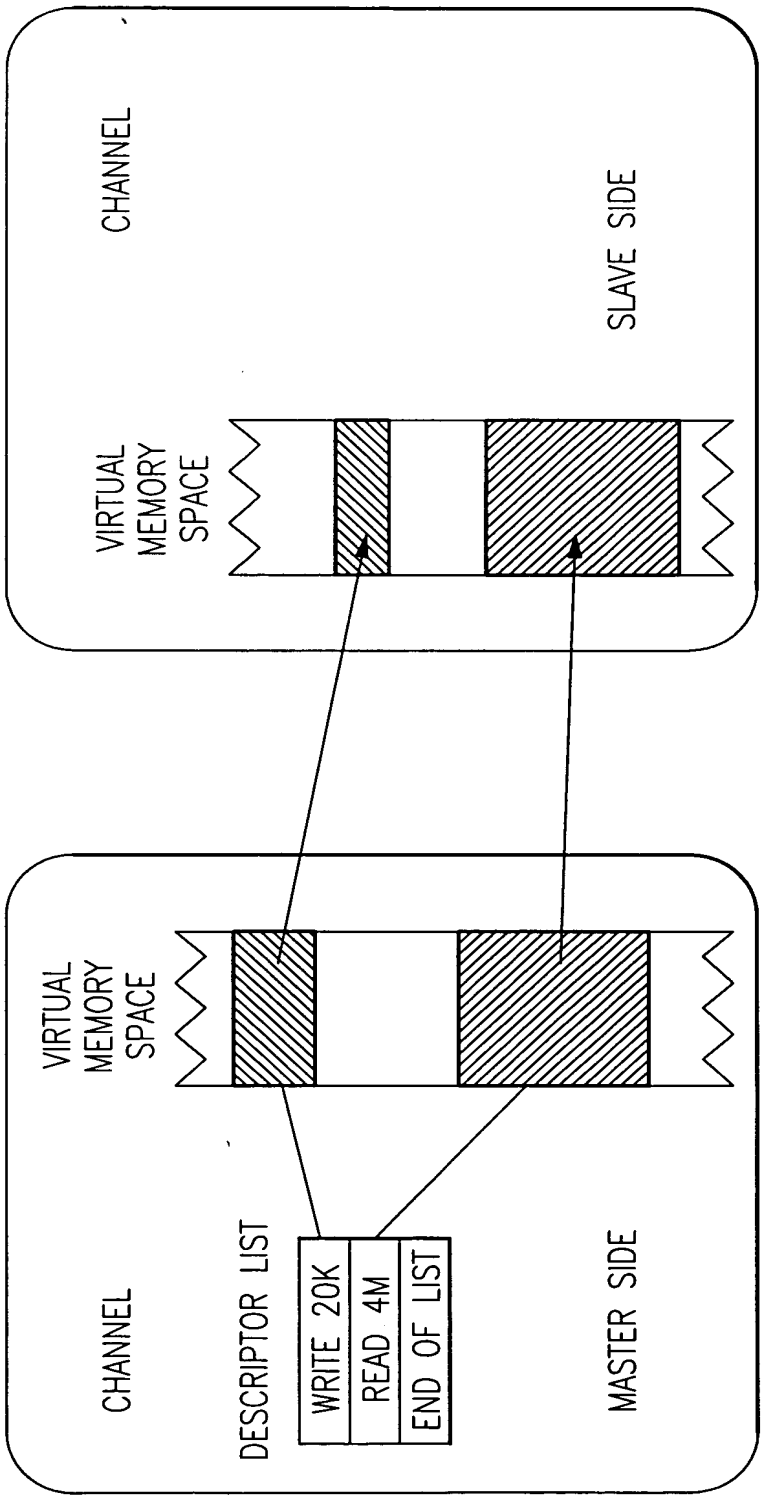
CHANNEL
VIRTUAL MEMORY SPACE
SLAVE SIDE
CHANNEL
VIRTUAL MEMORY SPACE
DESCRIPTOR LIST
WRITE 20K
READ 4M
END OF LIST
MASTER SIDE

FIG.5

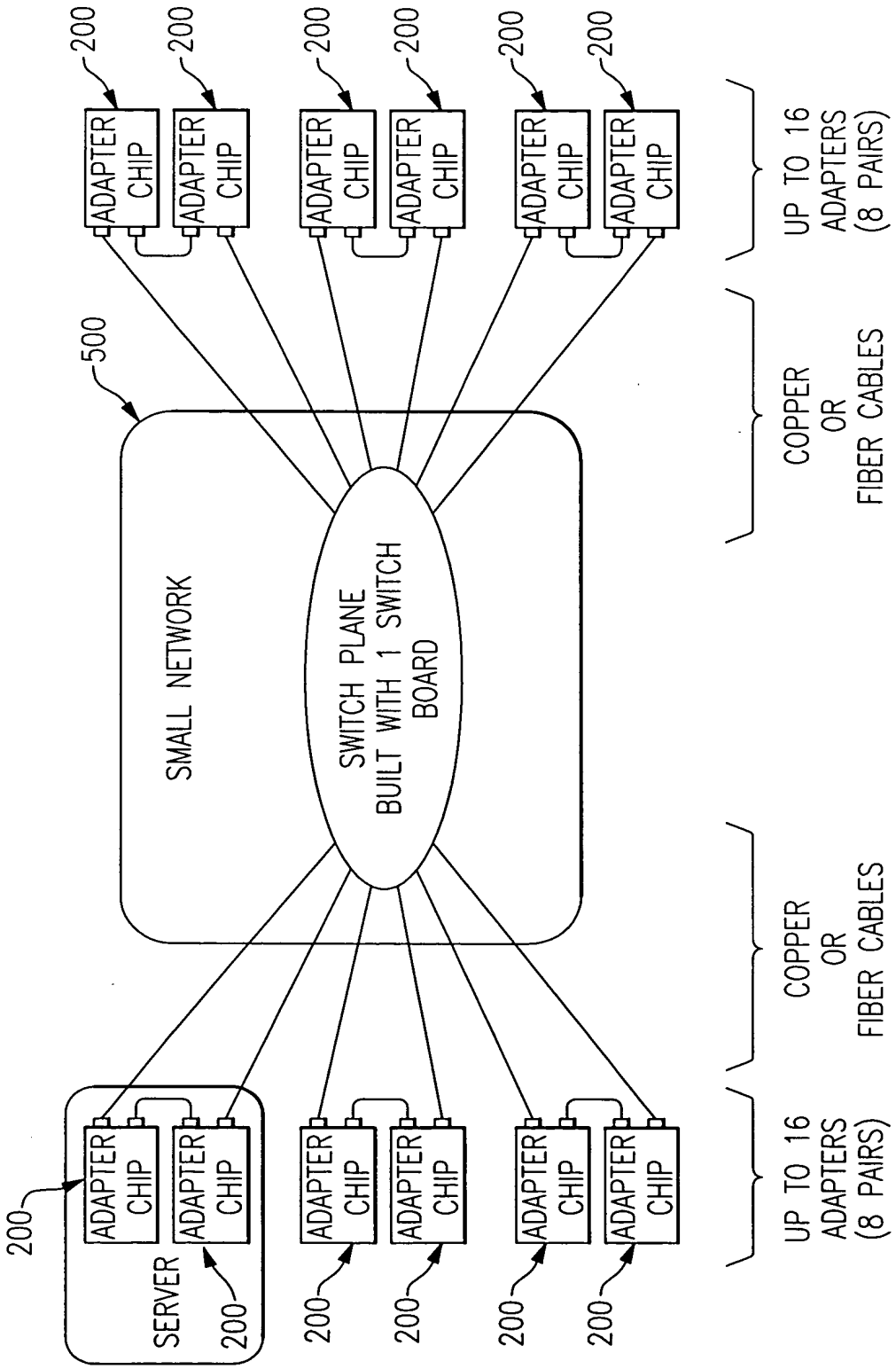
200
ADAPTER CHIP
ADAPTER CHIP
SERVER
200
500
SMALL NETWORK
SWITCH PLANE BUILT WITH 1 SWITCH BOARD
UP TO 16 ADAPTERS (8 PAIRS)
COPPER OR FIBER CABLES
UP TO 16 ADAPTERS (8 PAIRS)
COPPER OR FIBER CABLES

FIG.6

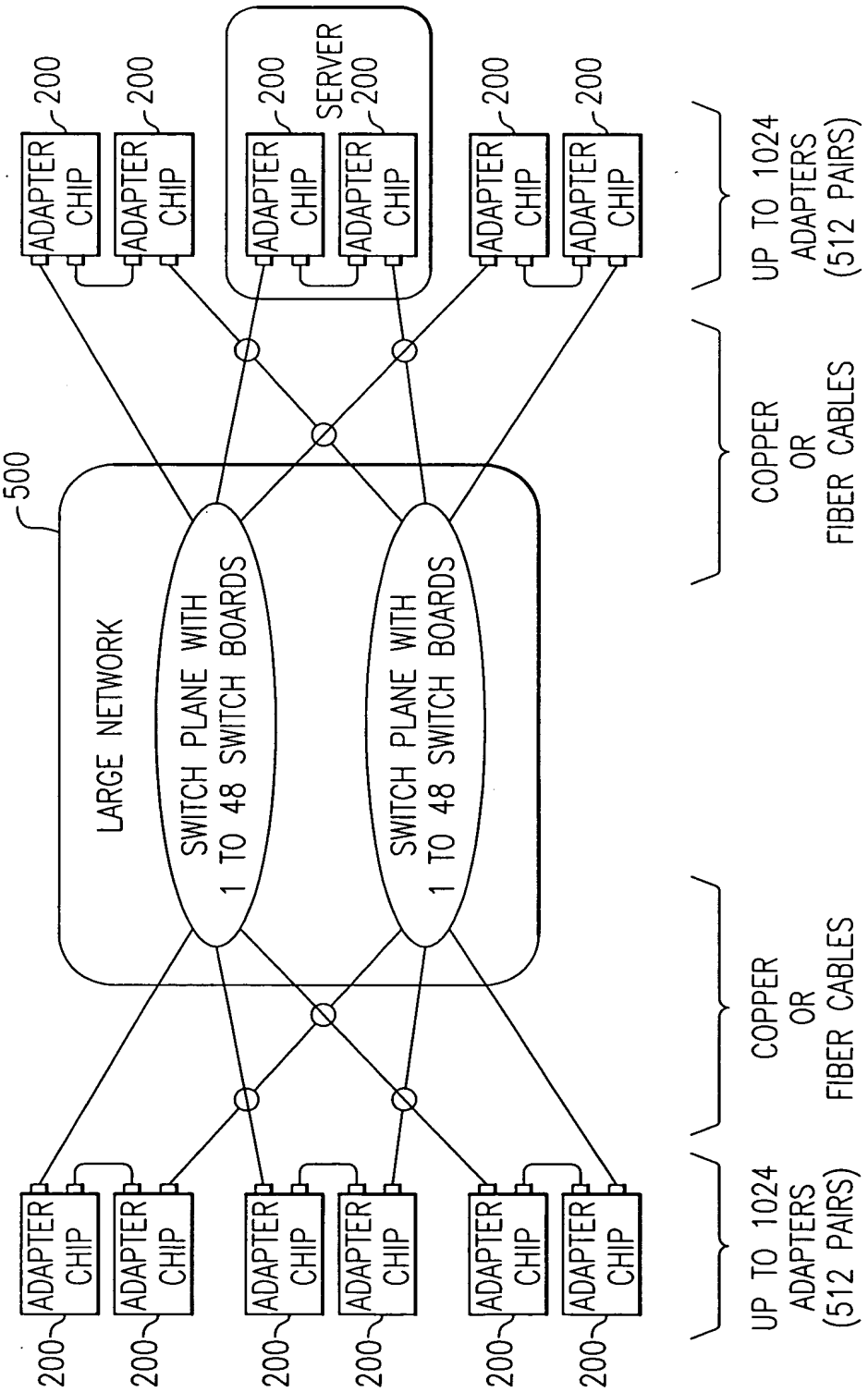
500
LARGE NETWORK
SWITCH PLANE WITH
1 TO 48 SWITCH BOARDS
SWITCH PLANE WITH
1 TO 48 SWITCH BOARDS
SERVER
ADAPTER
CHIP
200
UP TO 1024
ADAPTERS
(512 PAIRS)
COPPER
OR
FIBER CABLES

FIG.7

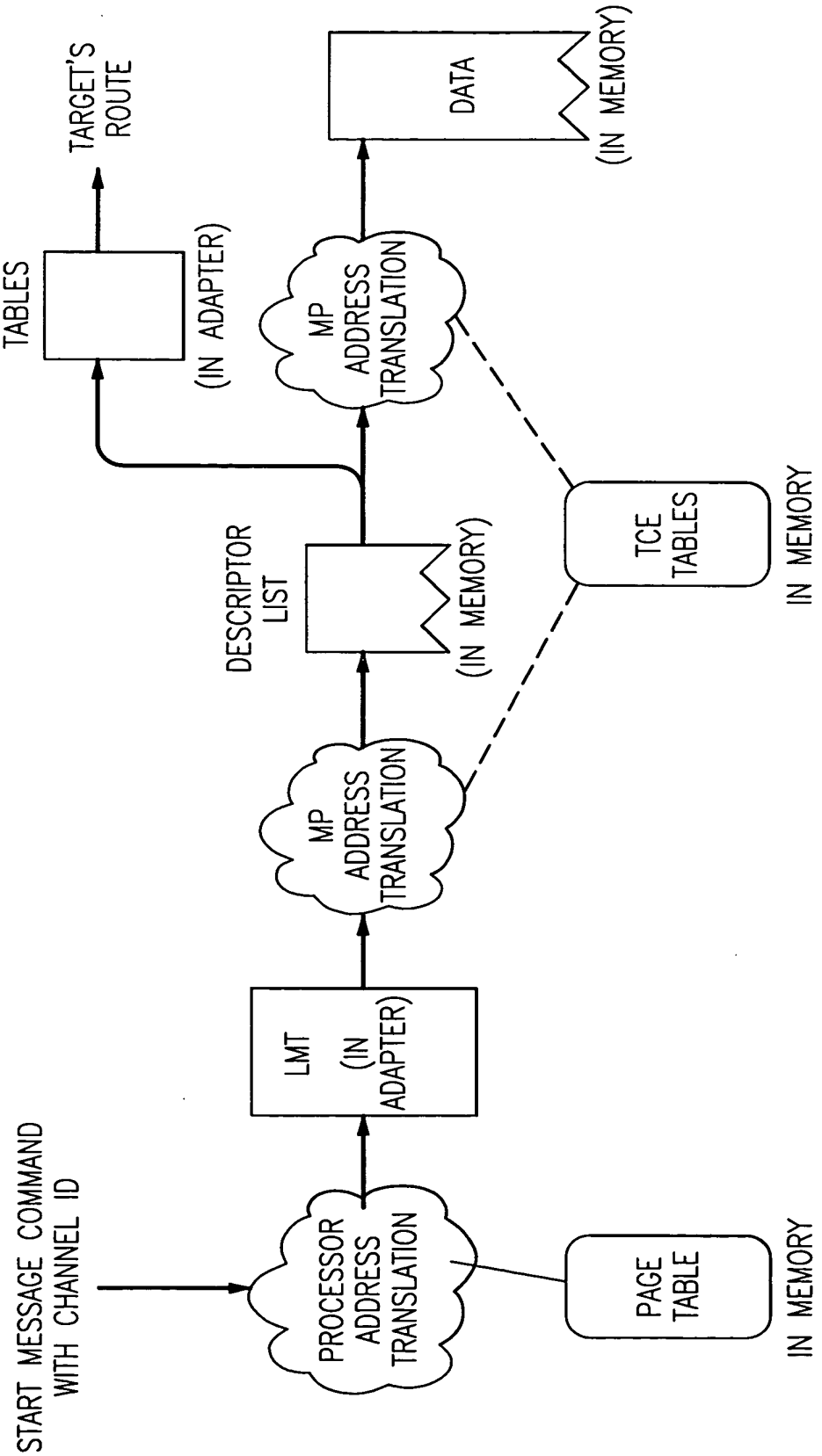
START MESSAGE COMMAND WITH CHANNEL ID
PROCESSOR ADDRESS TRANSLATION
PAGE TABLE
IN MEMORY
LMT (IN ADAPTER)
MP ADDRESS TRANSLATION
MP ADDRESS TRANSLATION
DESCRIPTOR LIST
(IN MEMORY)
TCE TABLES
IN MEMORY
PATH & ROUTE TABLES
(IN ADAPTER)
TARGET'S ROUTE
DATA
(IN MEMORY)

FIG.8

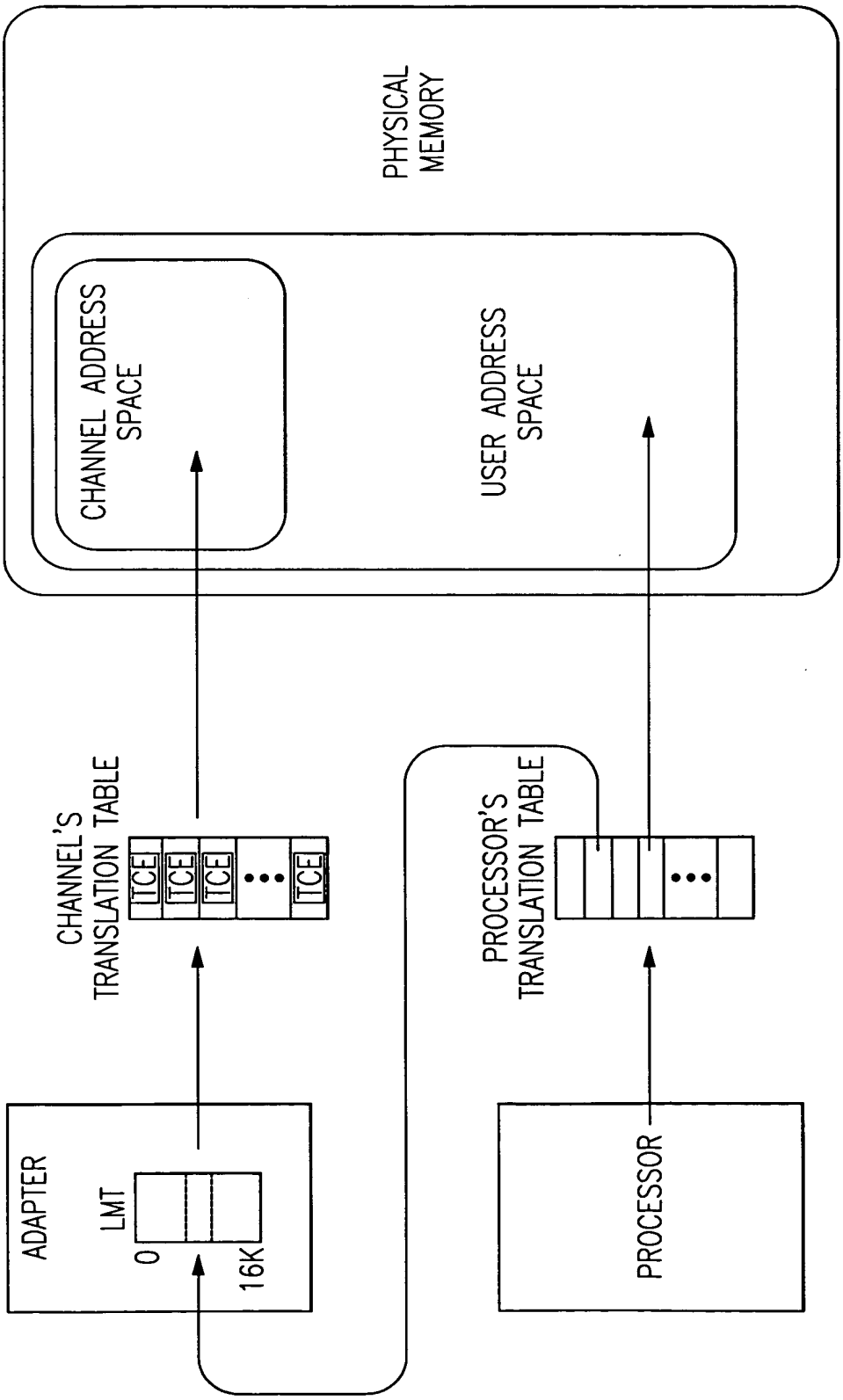
PHYSICAL MEMORY
CHANNEL ADDRESS SPACE
USER ADDRESS SPACE
CHANNEL'S TRANSLATION TABLE
TCE
TCE
TCE
TCE
PROCESSOR'S TRANSLATION TABLE
ADAPTER
LMT
0
16K
PROCESSOR

FIG.9

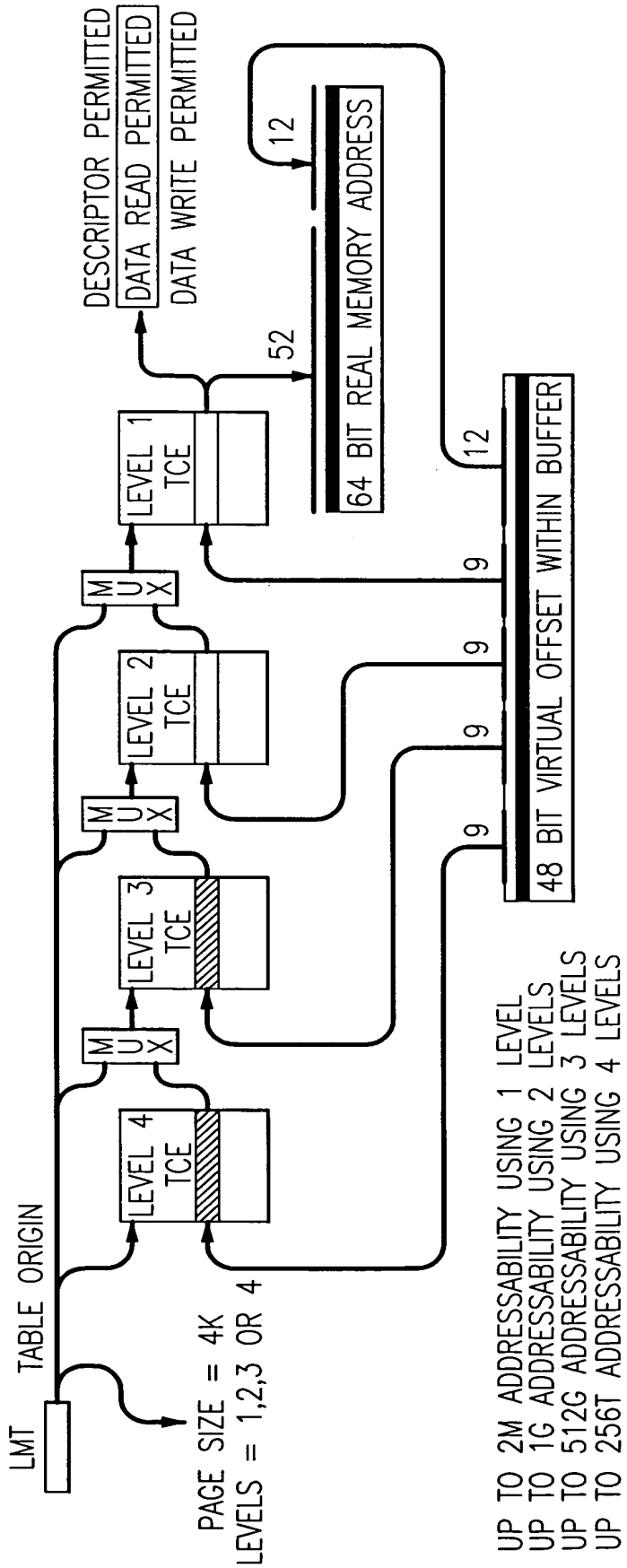
LMT
TABLE ORIGIN
PAGE SIZE = 4K
LEVELS = 1,2,3 OR 4
LEVEL 4 TCE
LEVEL 3 TCE
LEVEL 2 TCE
LEVEL 1 TCE
MUX
MUX
MUX
DESCRIPTOR PERMITTED
DATA READ PERMITTED
DATA WRITE PERMITTED
52
64 BIT REAL MEMORY ADDRESS
12
12
9
9
9
9
48 BIT VIRTUAL OFFSET WITHIN BUFFER
UP TO 2M ADDRESSABILITY USING 1 LEVEL
UP TO 1G ADDRESSABILITY USING 2 LEVELS
UP TO 512G ADDRESSABILITY USING 3 LEVELS
UP TO 256T ADDRESSABILITY USING 4 LEVELS

FIG.10

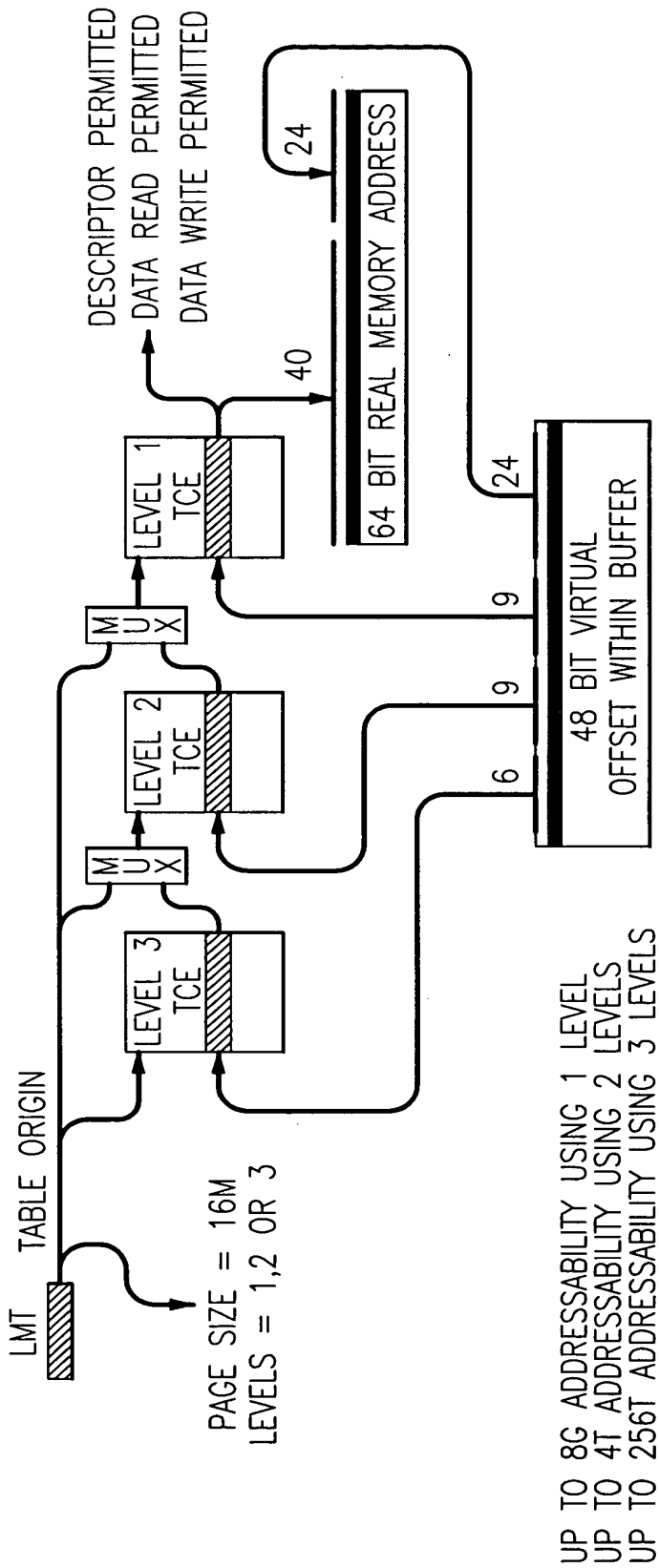
LMT
TABLE ORIGIN
PAGE SIZE = 16M
LEVELS = 1,2 OR 3
LEVEL 3 TCE
LEVEL 2 TCE
LEVEL 1 TCE
MUX
MUX
DESCRIPTOR PERMITTED
DATA READ PERMITTED
DATA WRITE PERMITTED
40
64 BIT REAL MEMORY ADDRESS
24
24
9
9
6
48 BIT VIRTUAL
OFFSET WITHIN BUFFER
UP TO 8G ADDRESSABILITY USING 1 LEVEL
UP TO 4T ADDRESSABILITY USING 2 LEVELS
UP TO 256T ADDRESSABILITY USING 3 LEVELS

FIG.11

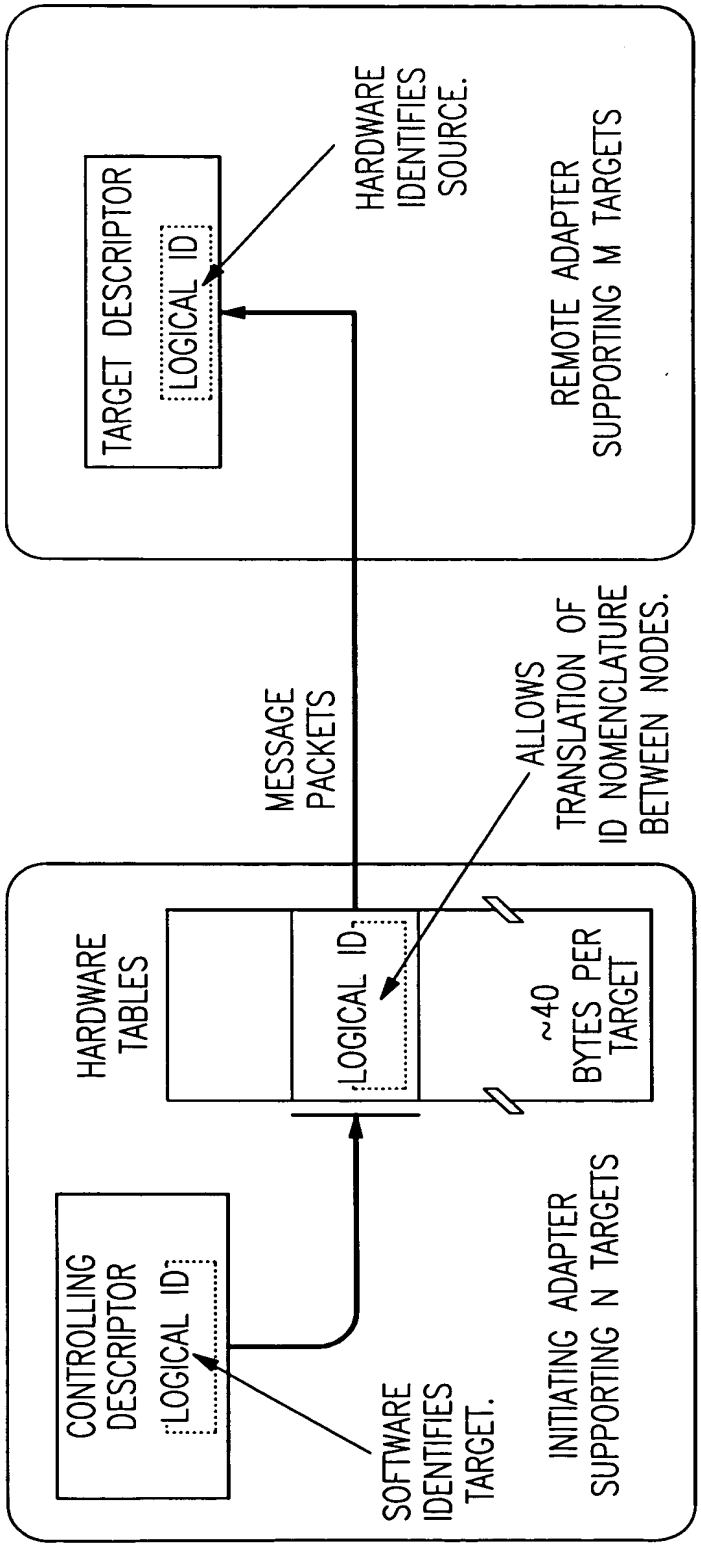
TARGET DESCRIPTOR
LOGICAL ID
HARDWARE IDENTIFIES SOURCE.
REMOTE ADAPTER SUPPORTING M TARGETS
MESSAGE PACKETS
ALLOWS TRANSLATION OF ID NOMENCLATURE BETWEEN NODES.
HARDWARE TABLES
LOGICAL ID
~40 BYTES PER TARGET
CONTROLLING DESCRIPTOR
LOGICAL ID
SOFTWARE IDENTIFIES TARGET.
INITIATING ADAPTER SUPPORTING N TARGETS

FIG.12

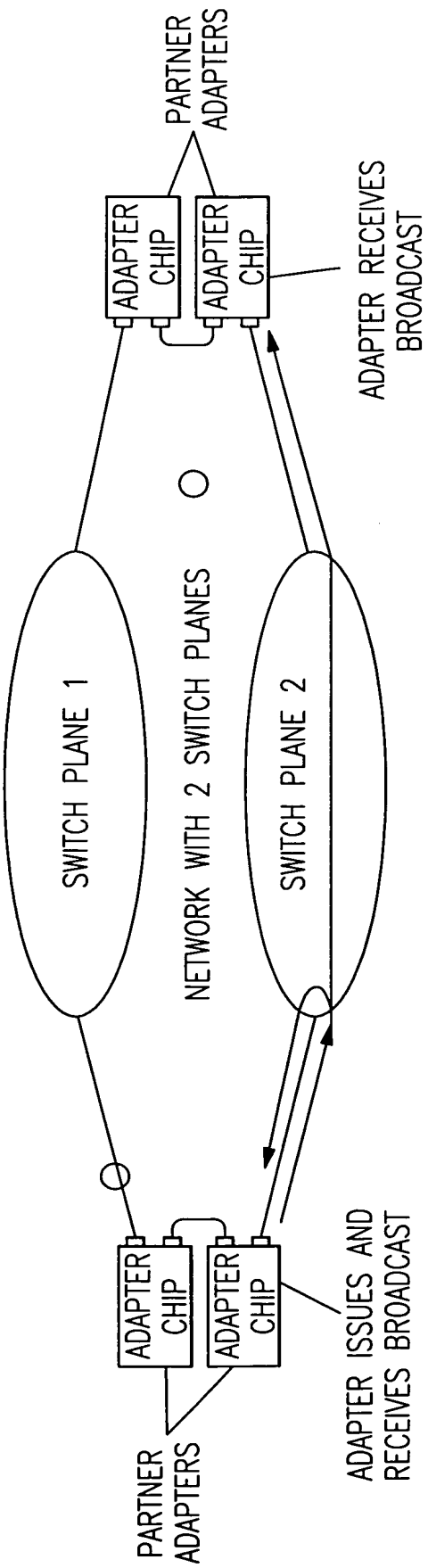
PARTNER ADAPTERS
ADAPTER CHIP
ADAPTER CHIP
ADAPTER RECEIVES BROADCAST
SWITCH PLANE 1
NETWORK WITH 2 SWITCH PLANES
SWITCH PLANE 2
ADAPTER CHIP
ADAPTER CHIP
ADAPTER ISSUES AND RECEIVES BROADCAST
PARTNER ADAPTERS

FIG.13

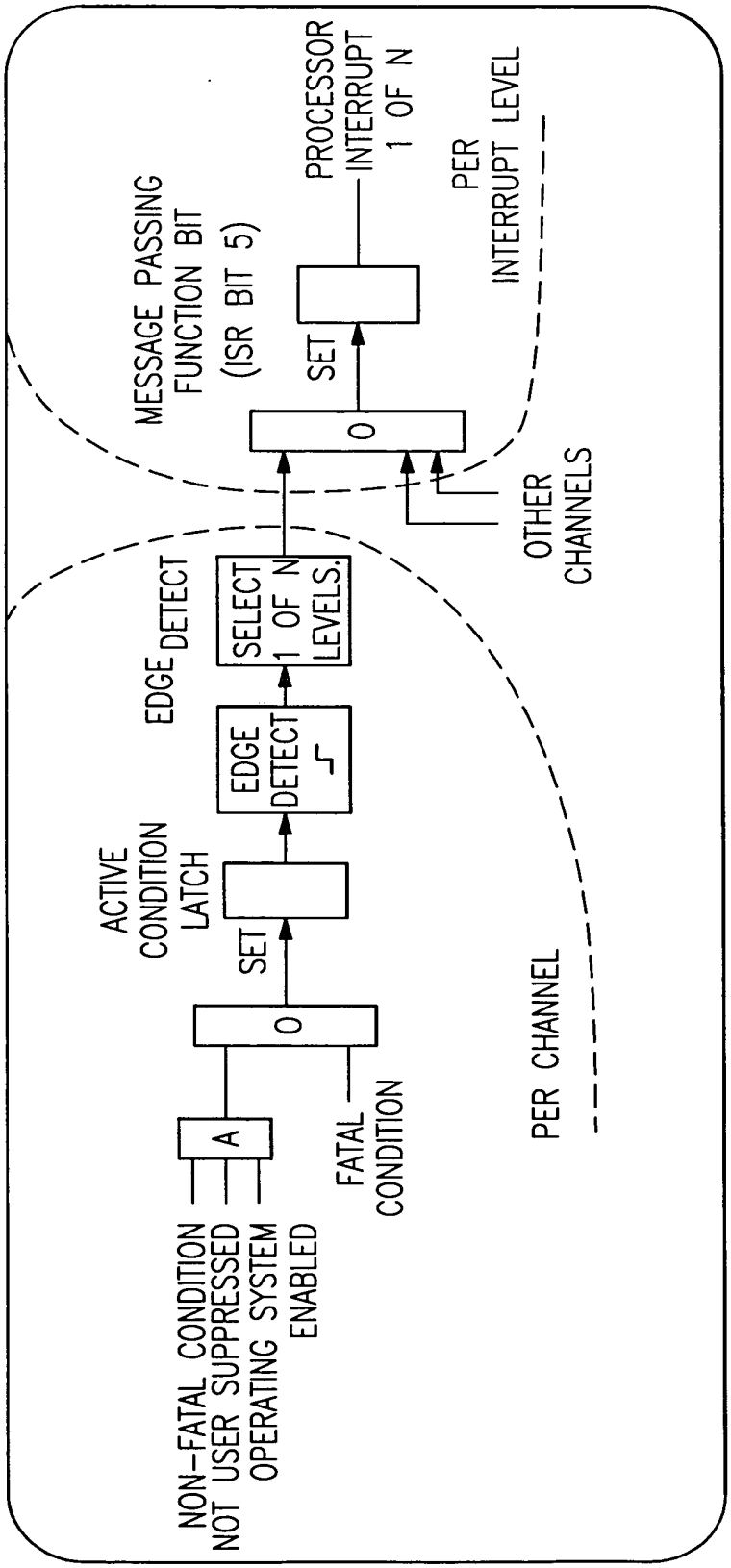
NON-FATAL CONDITION NOT USER SUPPRESSED OPERATING SYSTEM ENABLED
A
FATAL CONDITION
0
SET
ACTIVE CONDITION LATCH
EDGE DETECT
EDGE DETECT
SELECT 1 OF N LEVELS.
PER CHANNEL
MESSAGE PASSING FUNCTION BIT (ISR BIT 5)
0
SET
PROCESSOR INTERRUPT 1 OF N
PER INTERRUPT LEVEL
OTHER CHANNELS

FIG.14

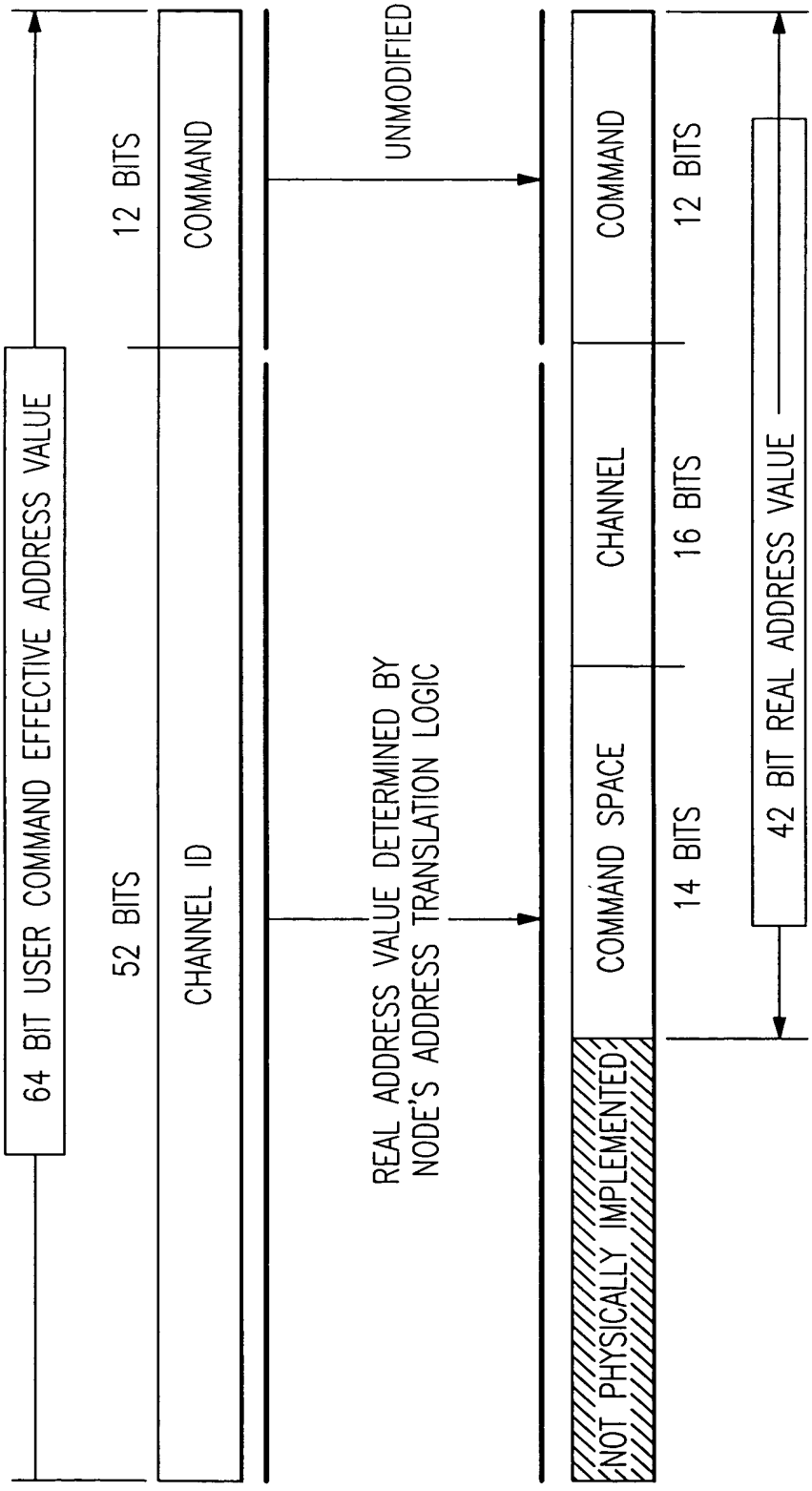
64 BIT USER COMMAND EFFECTIVE ADDRESS VALUE
52 BITS
CHANNEL ID
12 BITS
COMMAND
UNMODIFIED
REAL ADDRESS VALUE DETERMINED BY
NODE'S ADDRESS TRANSLATION LOGIC
NOT PHYSICALLY IMPLEMENTED
14 BITS
COMMAND SPACE
16 BITS
CHANNEL
12 BITS
COMMAND
42 BIT REAL ADDRESS VALUE

FIG.15

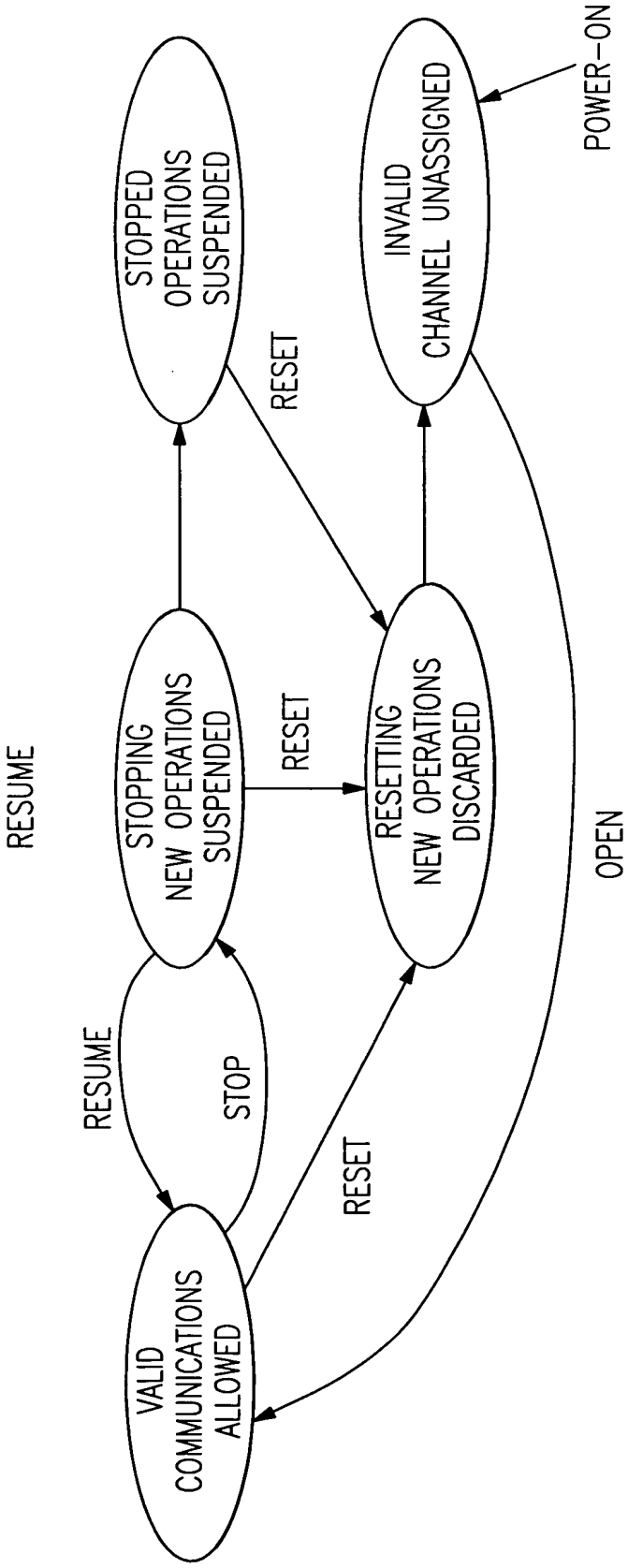
STOPPED OPERATIONS SUSPENDED
INVALID CHANNEL UNASSIGNED
POWER-ON
RESET
STOPPING NEW OPERATIONS SUSPENDED
RESETTING NEW OPERATIONS DISCARDED
RESUME
RESET
RESUME
STOP
RESET
OPEN
VALID COMMUNICATIONS ALLOWED

FIG.16

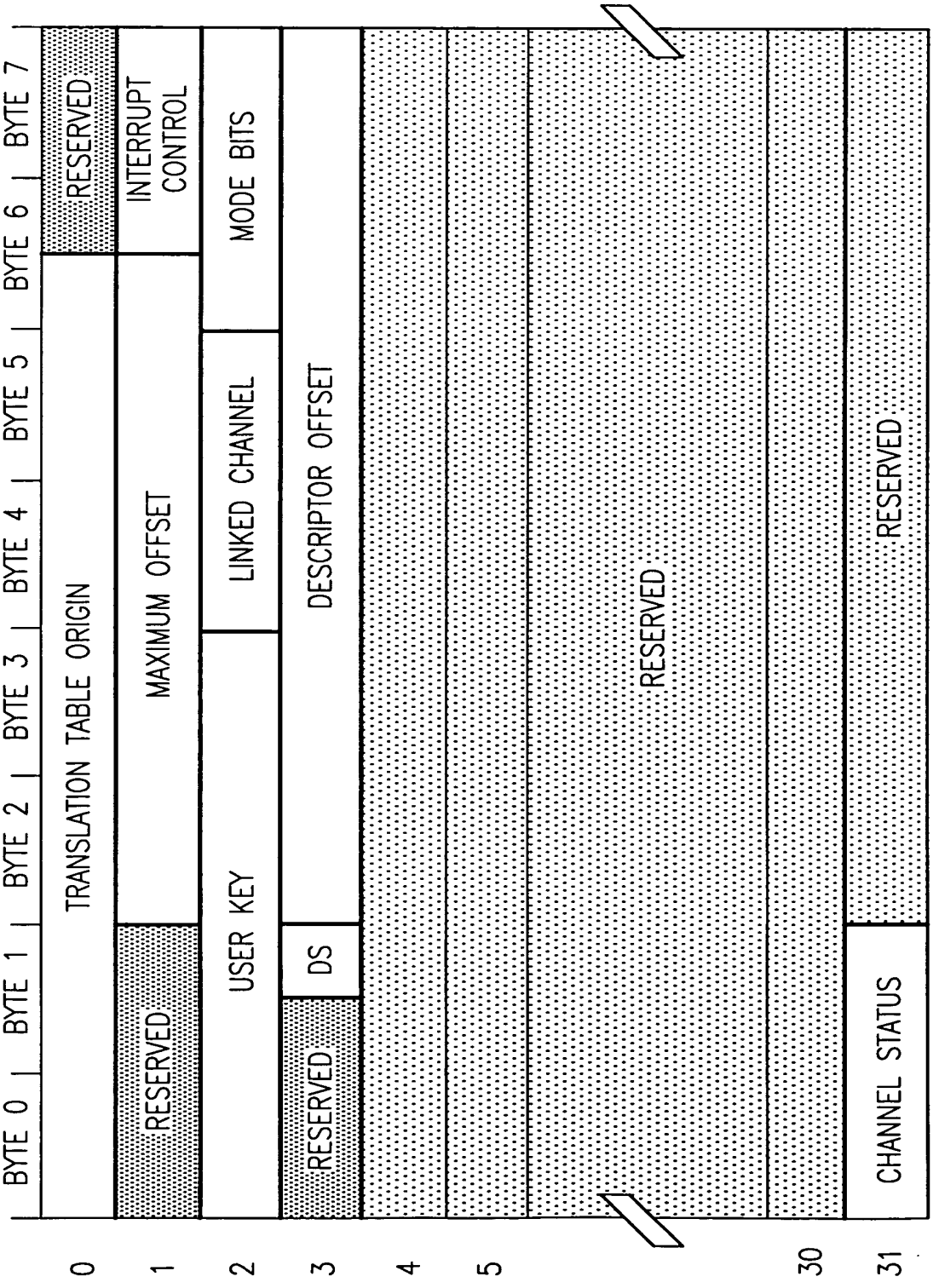
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
BYTE 6
BYTE 7
TRANSLATION TABLE ORIGIN
RESERVED
RESERVED
MAXIMUM OFFSET
INTERRUPT CONTROL
USER KEY
LINKED CHANNEL
MODE BITS
RESERVED
DS
DESCRIPTOR OFFSET
RESERVED
CHANNEL STATUS
RESERVED
0
1
2
3
4
5
30
31

FIG.17


TCE FORMAT
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
BYTE 6
BYTE 7
PAGE POINTER
FLAGS

FIG.18

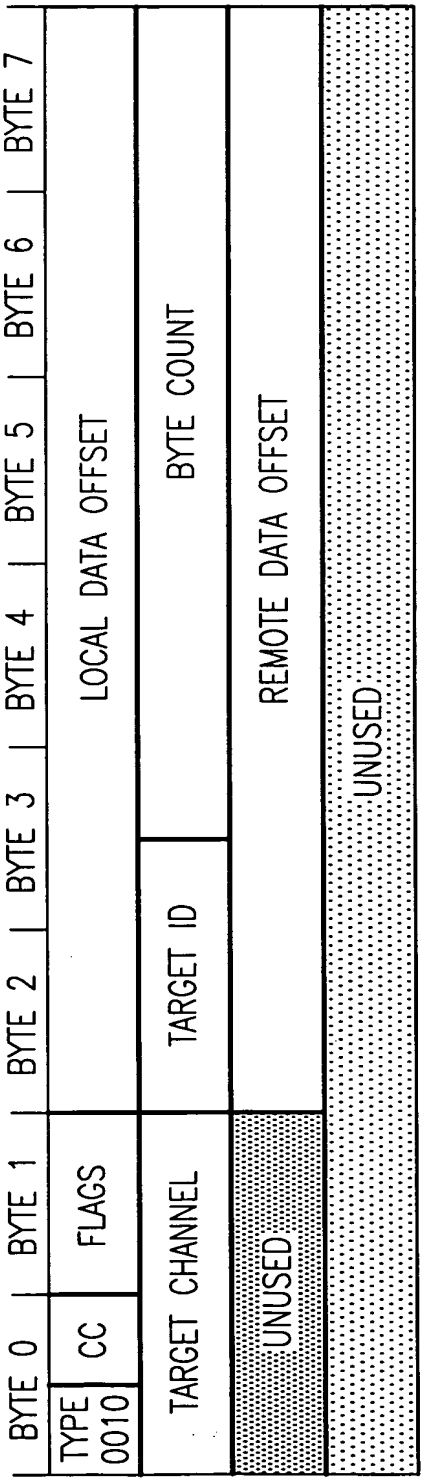
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
BYTE 6
BYTE 7
TYPE 0010
CC
FLAGS
LOCAL DATA OFFSET
TARGET CHANNEL
TARGET ID
BYTE COUNT
UNUSED
REMOTE DATA OFFSET
UNUSED
BYTES 0-7
BYTES 8-15
BYTES 16-23
BYTES 24-31

FIG.19

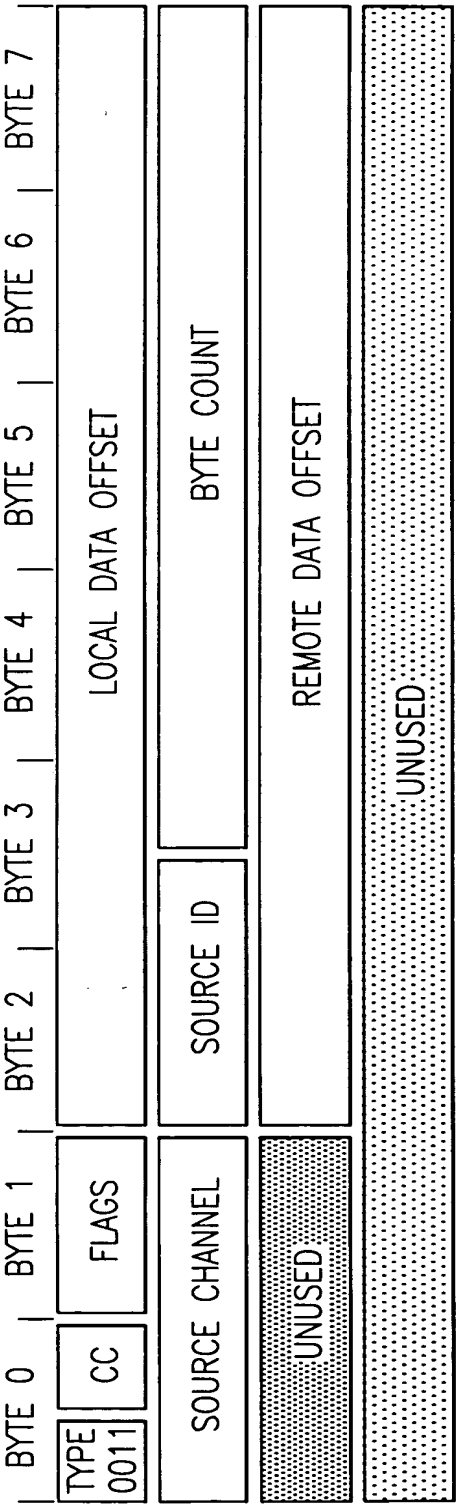
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
BYTE 6
BYTE 7
BYTES 0-7
TYPE 0011
CC
FLAGS
LOCAL DATA OFFSET
BYTES 8-15
SOURCE CHANNEL
SOURCE ID
BYTE COUNT
BYTES 16-23
UNUSED
REMOTE DATA OFFSET
BYTES 24-31
UNUSED

FIG.20

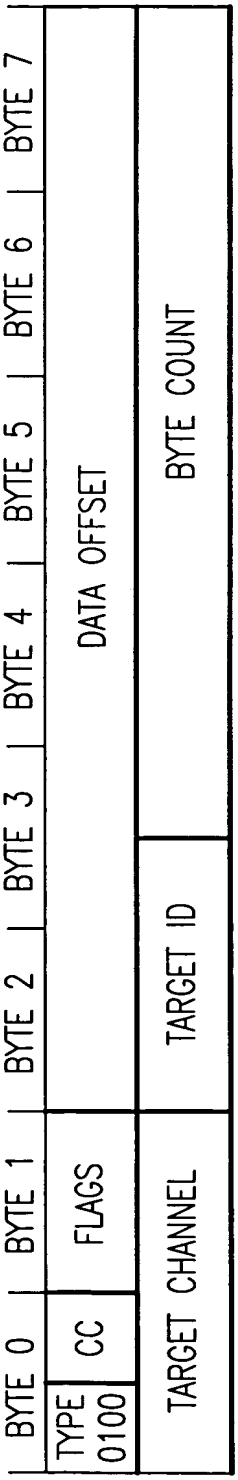
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
BYTE 6
BYTE 7
BYTES 0-7
TYPE 0100
CC
FLAGS
DATA OFFSET
BYTES 8-15
TARGET CHANNEL
TARGET ID
BYTE COUNT

FIG.21

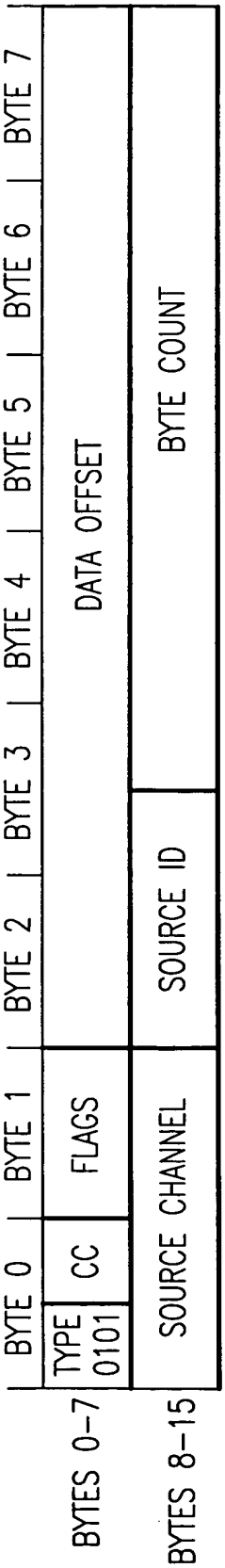
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
BYTE 6
BYTE 7
TYPE 0101
CC
FLAGS
DATA OFFSET
BYTES 0–7
SOURCE CHANNEL
SOURCE ID
BYTE COUNT
BYTES 8–15

FIG.22

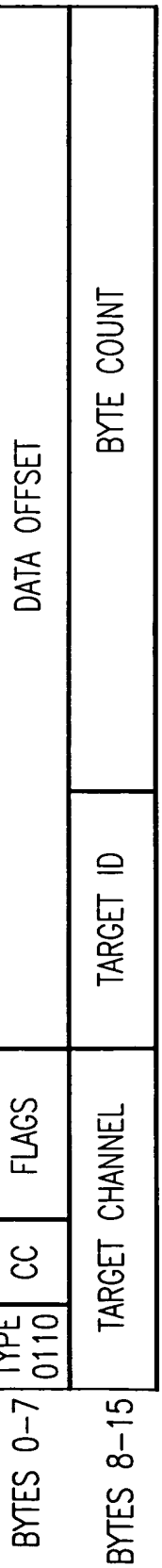
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
BYTE 6
BYTE 7
TYPE 0110
CC
FLAGS
DATA OFFSET
BYTES 0–7
TARGET CHANNEL
TARGET ID
BYTE COUNT
BYTES 8–15

FIG.23

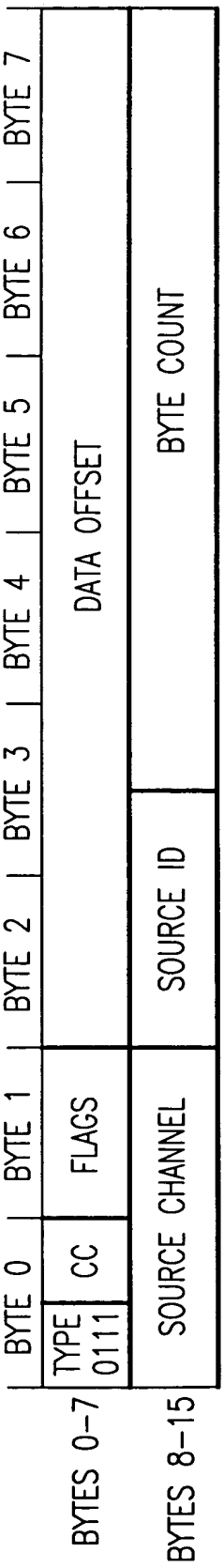
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
BYTE 6
BYTE 7
TYPE 0111
CC
FLAGS
DATA OFFSET
SOURCE CHANNEL
SOURCE ID
BYTE COUNT
BYTES 0–7
BYTES 8–15

FIG.24

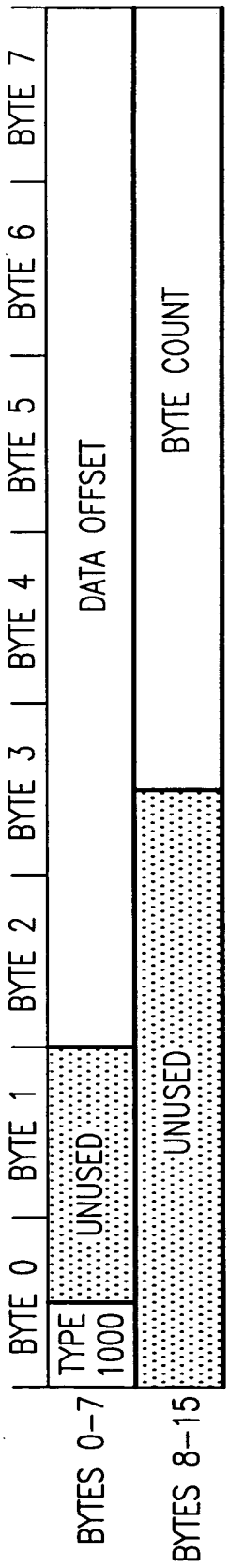
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
BYTE 6
BYTE 7
TYPE 1000
UNUSED
DATA OFFSET
UNUSED
BYTE COUNT
BYTES 0–7
BYTES 8–15

FIG.25

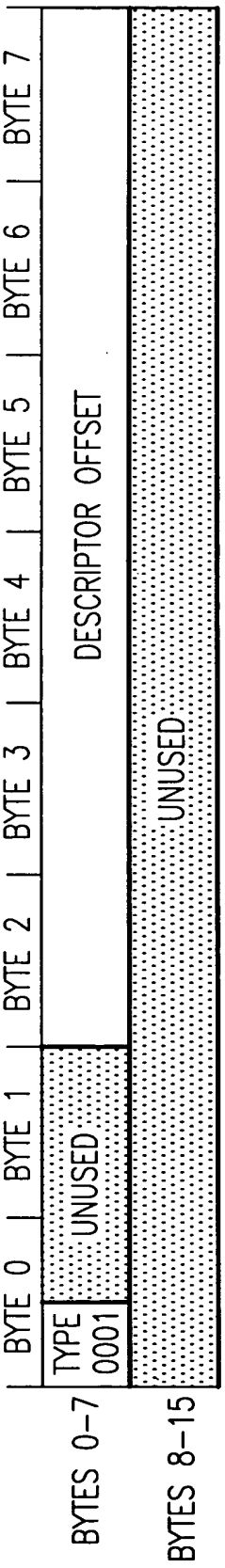
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
BYTE 6
BYTE 7
TYPE 0001
UNUSED
DESCRIPTOR OFFSET
UNUSED
BYTES 0–7
BYTES 8–15

FIG.26

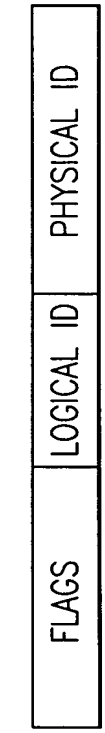
FLAGS
LOGICAL ID
PHYSICAL ID
LOGICAL ID
FROM DESCRIPTOR
OR DMA PACKET

FIG.27

	BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
PATH 0	0000	ROUTE NIBBLES						PORT
PATH 1	0000	ROUTE NIBBLES						PORT
PATH 2	0000	ROUTE NIBBLES						PORT
PATH 3	0000	ROUTE NIBBLES						PORT

FIG.28

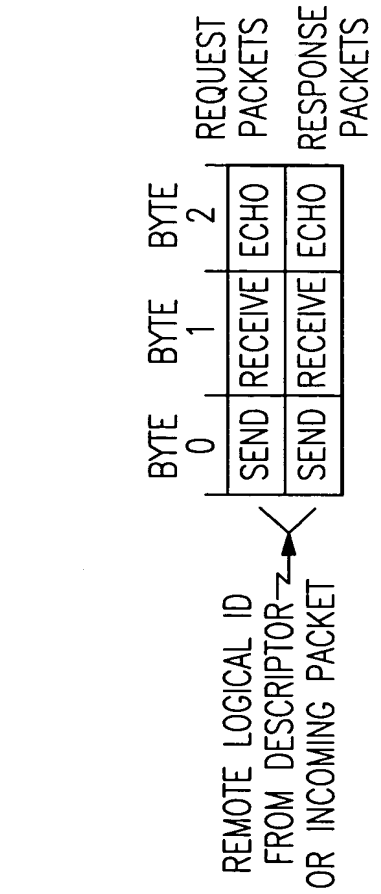

FIG.30

	BYTE 0	BYTE 1	BYTE 2
REGISTER 0	LOOKUP TABLE INDEX		PORT
REGISTER 1	LOOKUP TABLE INDEX		PORT
REGISTER 2	LOOKUP TABLE INDEX		PORT
REGISTER 3	LOOKUP TABLE INDEX		PORT

FIG.29

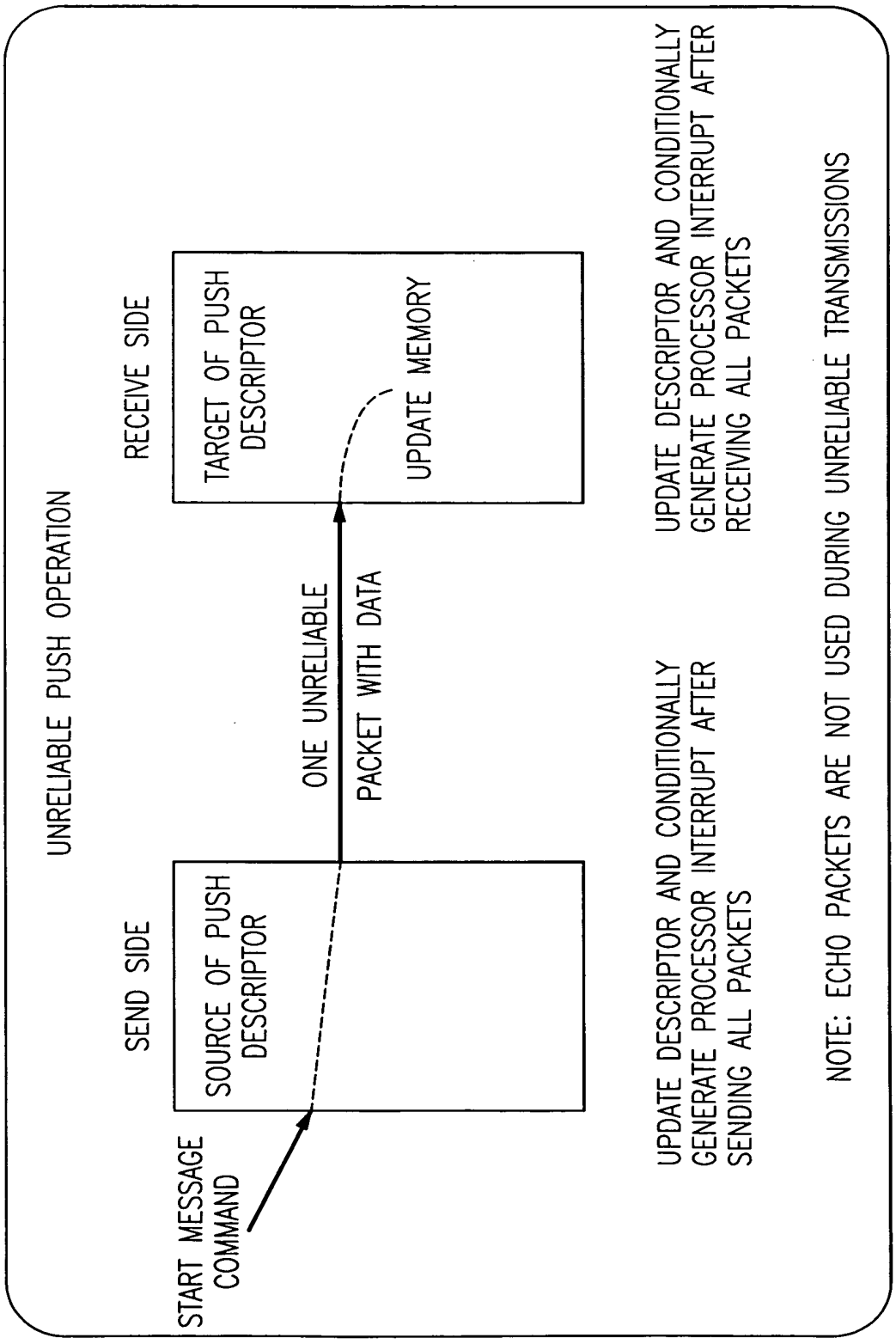
UNRELIABLE PUSH OPERATION
SEND SIDE
RECEIVE SIDE
START MESSAGE COMMAND
SOURCE OF PUSH DESCRIPTOR
ONE UNRELIABLE PACKET WITH DATA
TARGET OF PUSH DESCRIPTOR
UPDATE MEMORY
UPDATE DESCRIPTOR AND CONDITIONALLY GENERATE PROCESSOR INTERRUPT AFTER SENDING ALL PACKETS
UPDATE DESCRIPTOR AND CONDITIONALLY GENERATE PROCESSOR INTERRUPT AFTER RECEIVING ALL PACKETS
NOTE: ECHO PACKETS ARE NOT USED DURING UNRELIABLE TRANSMISSIONS

FIG.31

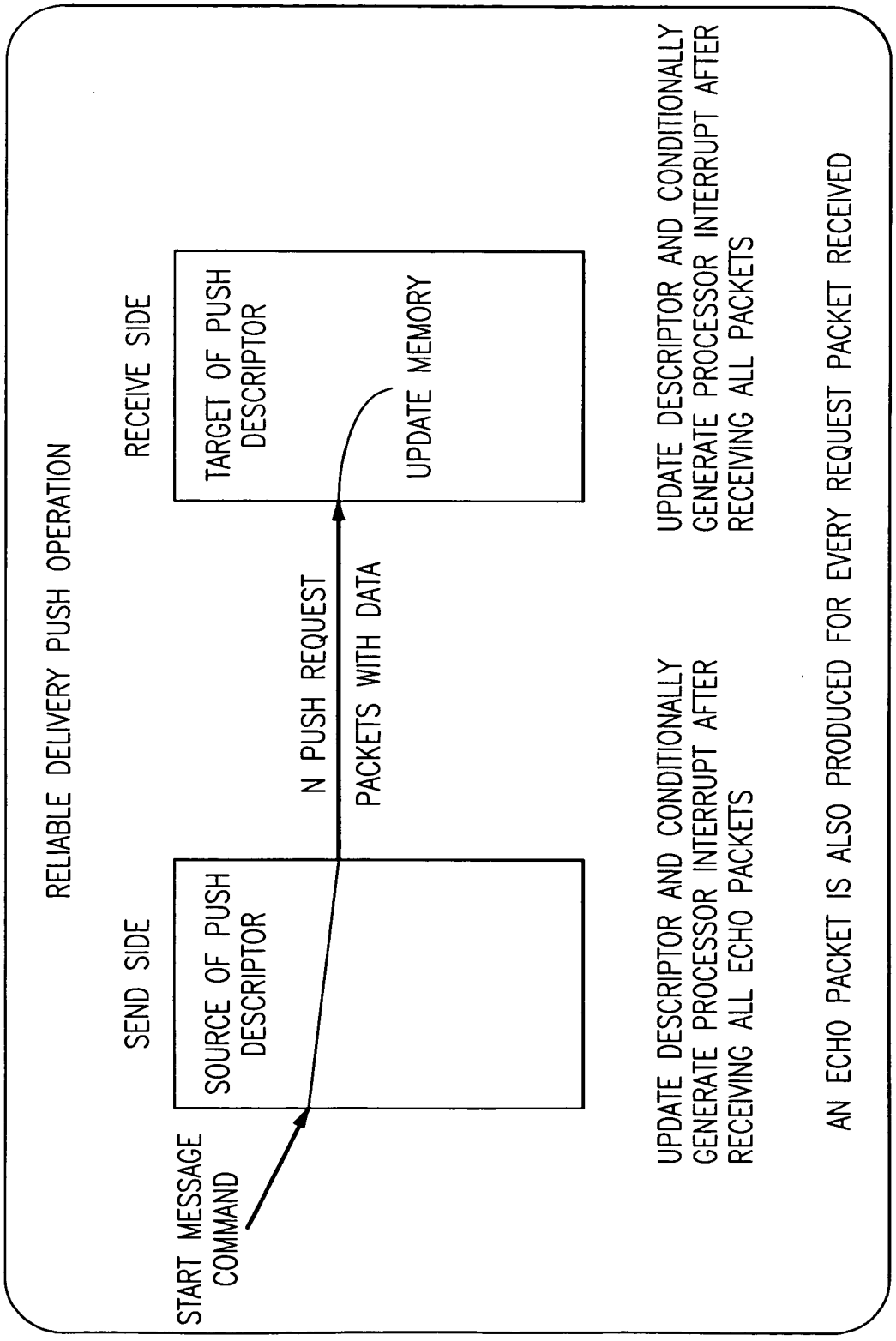
RELIABLE DELIVERY PUSH OPERATION
SEND SIDE
RECEIVE SIDE
SOURCE OF PUSH DESCRIPTOR
TARGET OF PUSH DESCRIPTOR
START MESSAGE COMMAND
N PUSH REQUEST
PACKETS WITH DATA
UPDATE MEMORY
UPDATE DESCRIPTOR AND CONDITIONALLY GENERATE PROCESSOR INTERRUPT AFTER RECEIVING ALL ECHO PACKETS
UPDATE DESCRIPTOR AND CONDITIONALLY GENERATE PROCESSOR INTERRUPT AFTER RECEIVING ALL PACKETS
AN ECHO PACKET IS ALSO PRODUCED FOR EVERY REQUEST PACKET RECEIVED

FIG.32

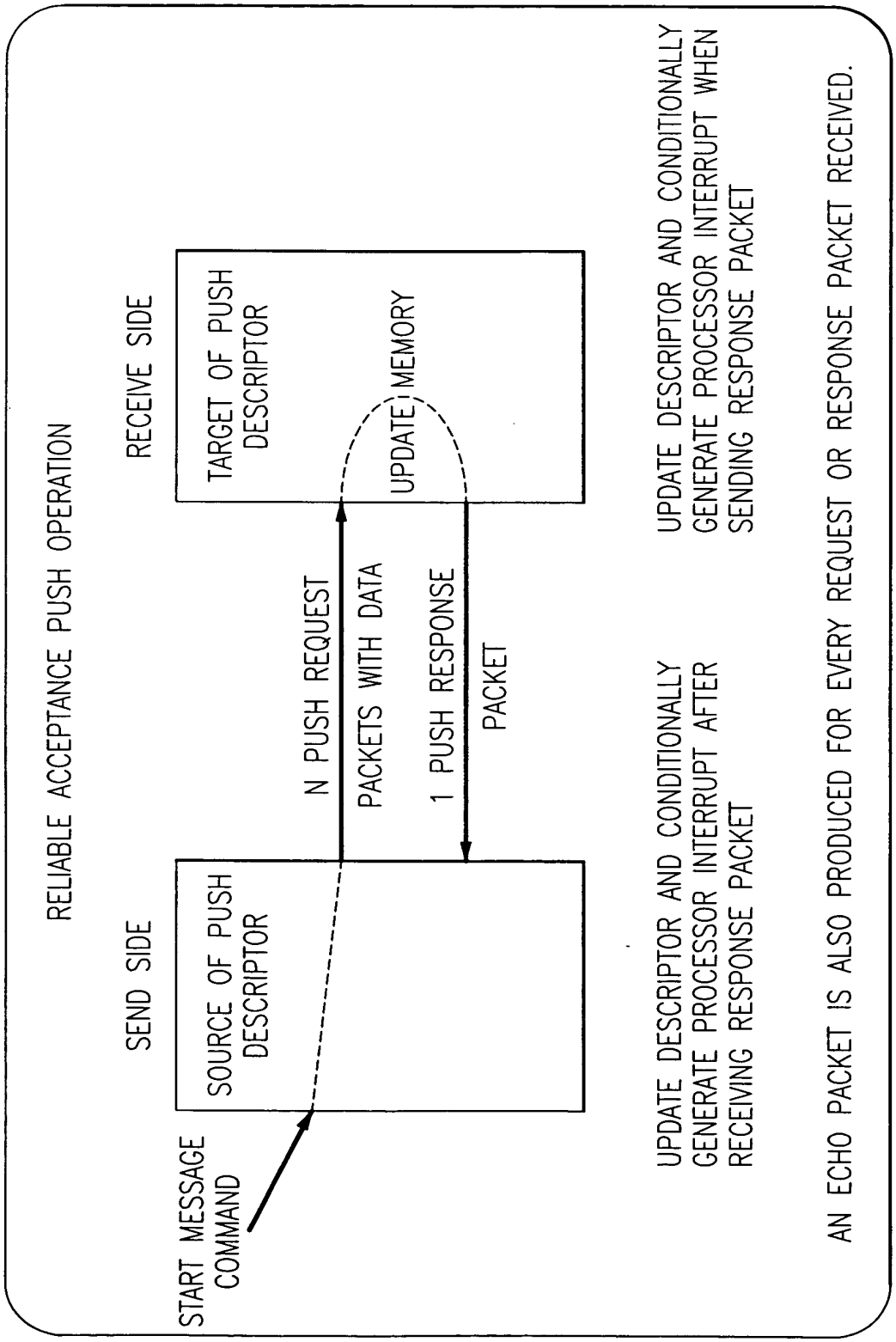
RELIABLE ACCEPTANCE PUSH OPERATION
SEND SIDE
RECEIVE SIDE
SOURCE OF PUSH DESCRIPTOR
TARGET OF PUSH DESCRIPTOR
START MESSAGE COMMAND
N PUSH REQUEST
PACKETS WITH DATA
1 PUSH RESPONSE PACKET
UPDATE MEMORY
UPDATE DESCRIPTOR AND CONDITIONALLY GENERATE PROCESSOR INTERRUPT AFTER RECEIVING RESPONSE PACKET
UPDATE DESCRIPTOR AND CONDITIONALLY GENERATE PROCESSOR INTERRUPT WHEN SENDING RESPONSE PACKET
AN ECHO PACKET IS ALSO PRODUCED FOR EVERY REQUEST OR RESPONSE PACKET RECEIVED.

FIG.33

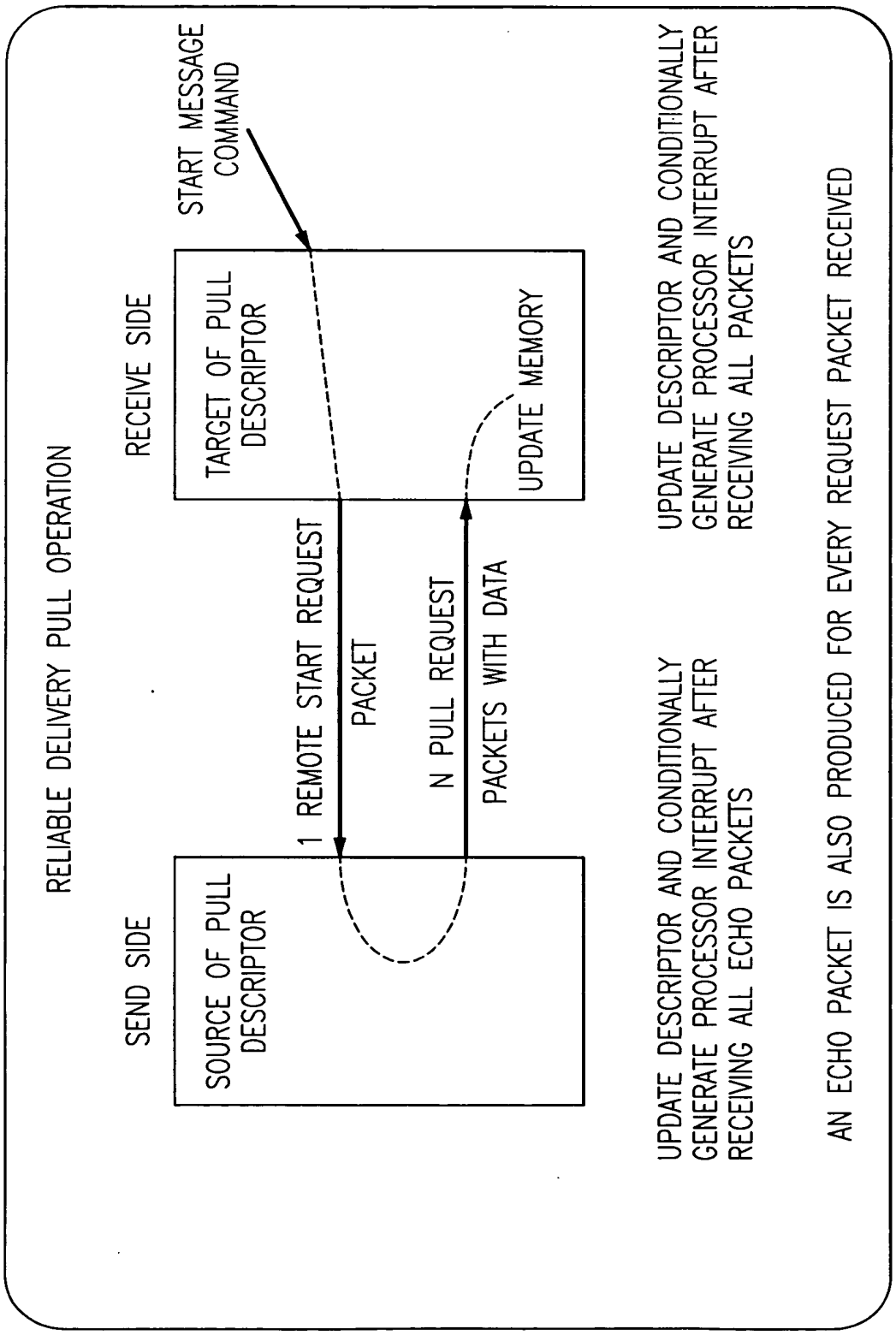
RELIABLE DELIVERY PULL OPERATION
SEND SIDE
RECEIVE SIDE
SOURCE OF PULL DESCRIPTOR
TARGET OF PULL DESCRIPTOR
START MESSAGE COMMAND
1 REMOTE START REQUEST
PACKET
N PULL REQUEST
PACKETS WITH DATA
UPDATE MEMORY
UPDATE DESCRIPTOR AND CONDITIONALLY GENERATE PROCESSOR INTERRUPT AFTER RECEIVING ALL ECHO PACKETS
UPDATE DESCRIPTOR AND CONDITIONALLY GENERATE PROCESSOR INTERRUPT AFTER RECEIVING ALL PACKETS
AN ECHO PACKET IS ALSO PRODUCED FOR EVERY REQUEST PACKET RECEIVED

FIG.34

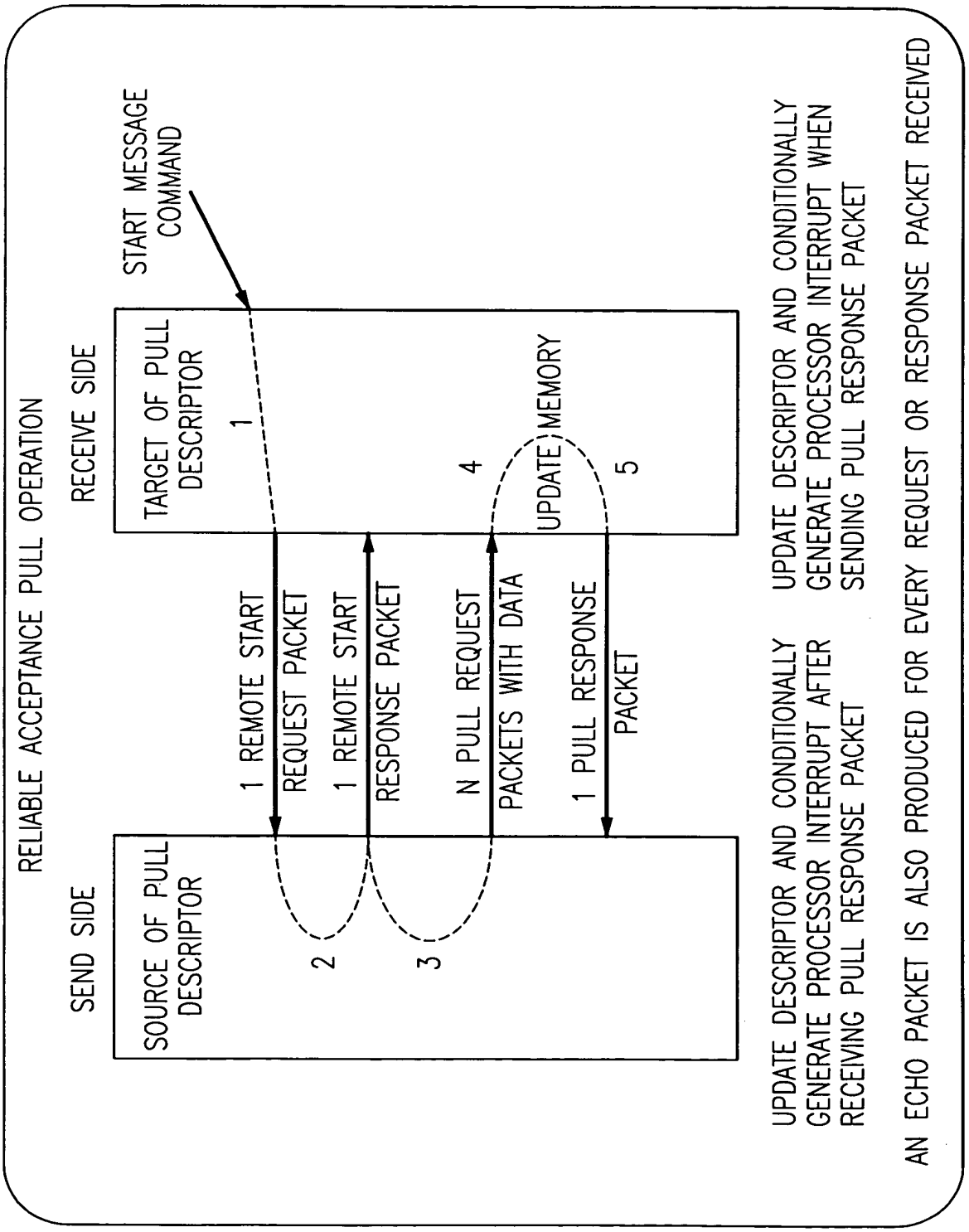
RELIABLE ACCEPTANCE PULL OPERATION
SEND SIDE
RECEIVE SIDE
SOURCE OF PULL DESCRIPTOR
TARGET OF PULL DESCRIPTOR
START MESSAGE COMMAND
1
1 REMOTE START REQUEST PACKET
2
1 REMOTE START RESPONSE PACKET
3
N PULL REQUEST PACKETS WITH DATA
4
UPDATE MEMORY
1 PULL RESPONSE PACKET
5
UPDATE DESCRIPTOR AND CONDITIONALLY GENERATE PROCESSOR INTERRUPT AFTER RECEIVING PULL RESPONSE PACKET
UPDATE DESCRIPTOR AND CONDITIONALLY GENERATE PROCESSOR INTERRUPT WHEN SENDING PULL RESPONSE PACKET
AN ECHO PACKET IS ALSO PRODUCED FOR EVERY REQUEST OR RESPONSE PACKET RECEIVED

FIG.35

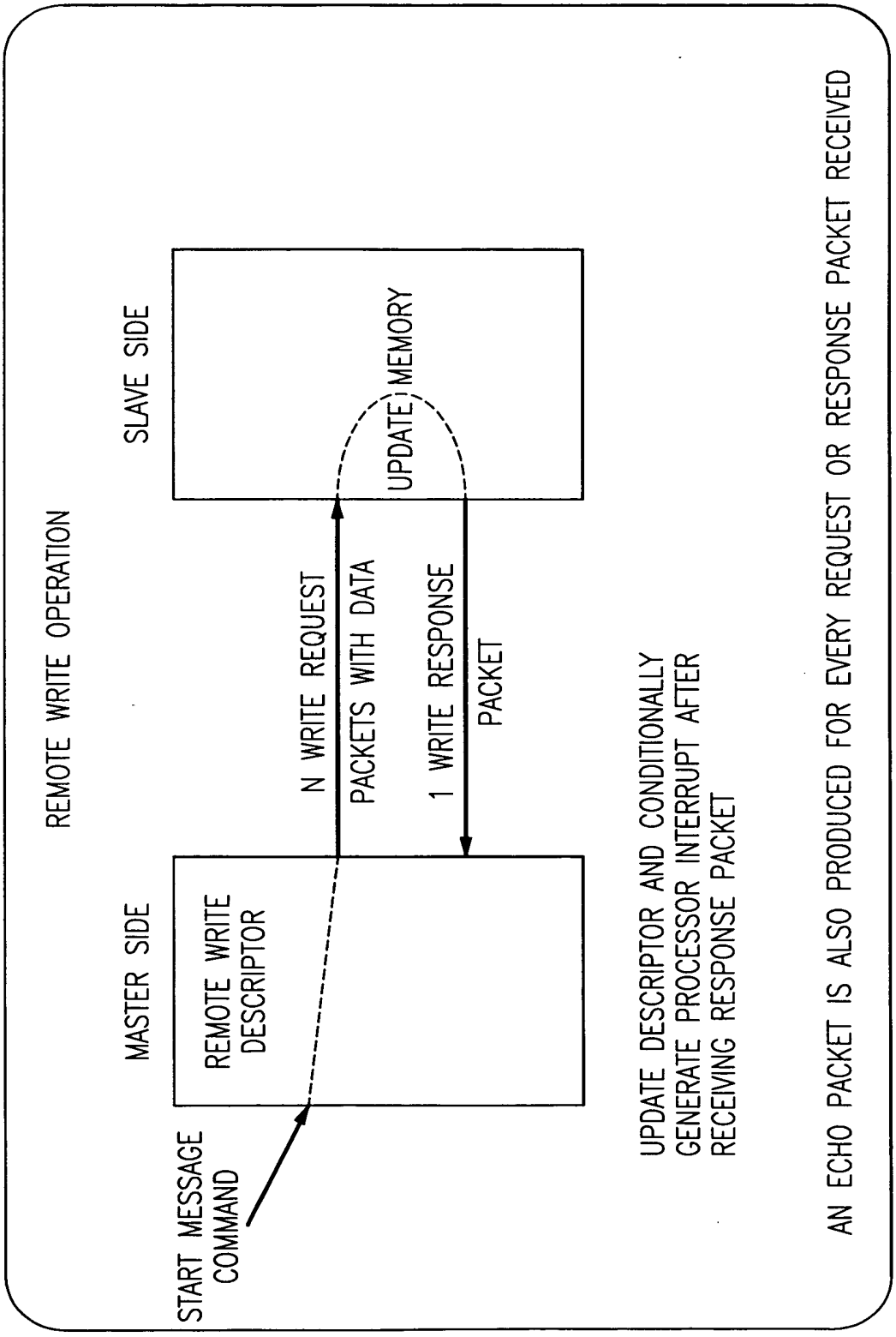
REMOTE WRITE OPERATION
MASTER SIDE
SLAVE SIDE
START MESSAGE COMMAND
REMOTE WRITE DESCRIPTOR
N WRITE REQUEST
PACKETS WITH DATA
1 WRITE RESPONSE
PACKET
UPDATE MEMORY
UPDATE DESCRIPTOR AND CONDITIONALLY
GENERATE PROCESSOR INTERRUPT AFTER
RECEIVING RESPONSE PACKET
AN ECHO PACKET IS ALSO PRODUCED FOR EVERY REQUEST OR RESPONSE PACKET RECEIVED

FIG.36

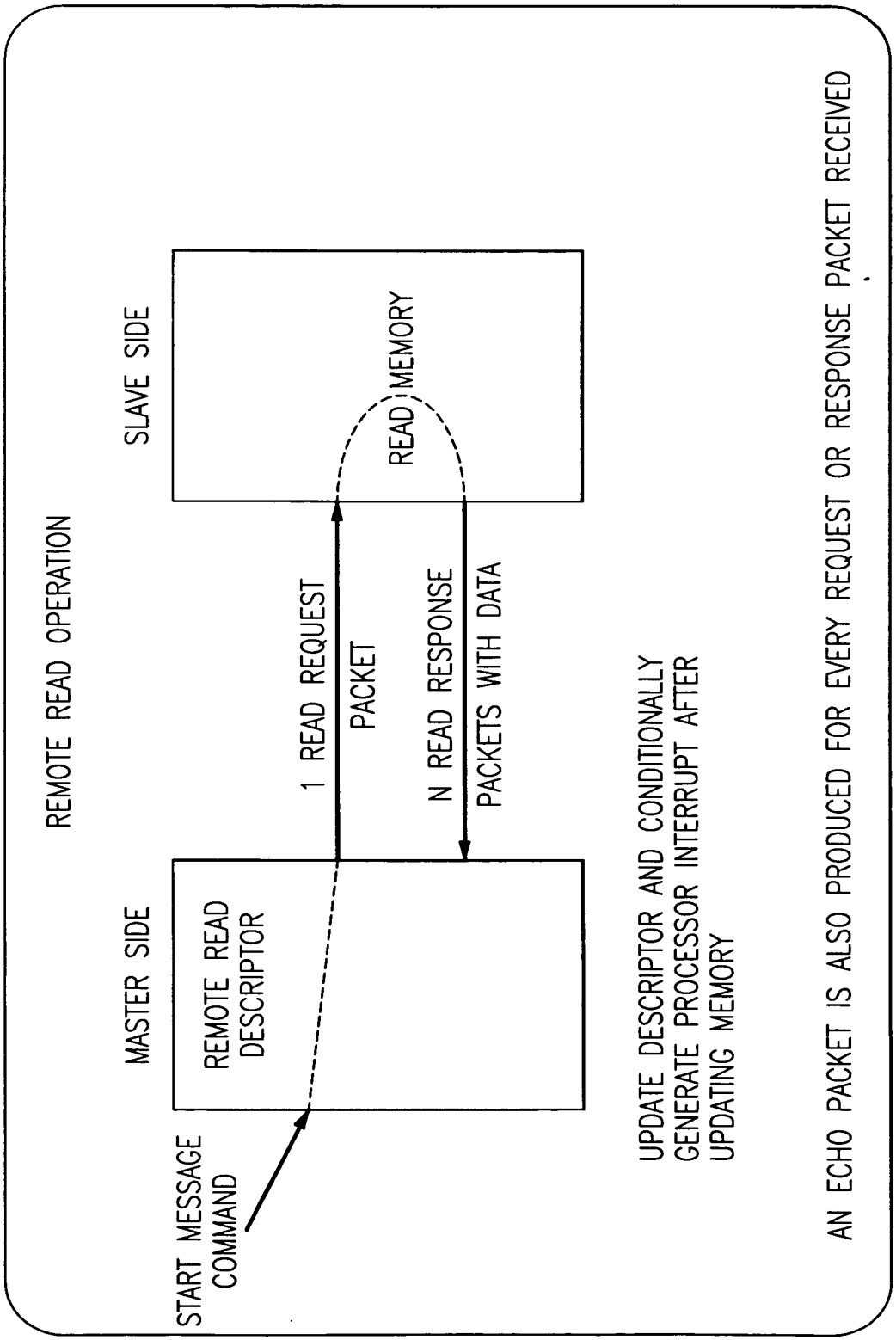
REMOTE READ OPERATION
MASTER SIDE
SLAVE SIDE
REMOTE READ DESCRIPTOR
START MESSAGE COMMAND
1 READ REQUEST PACKET
READ MEMORY
N READ RESPONSE PACKETS WITH DATA
UPDATE DESCRIPTOR AND CONDITIONALLY GENERATE PROCESSOR INTERRUPT AFTER UPDATING MEMORY
AN ECHO PACKET IS ALSO PRODUCED FOR EVERY REQUEST OR RESPONSE PACKET RECEIVED

FIG.37

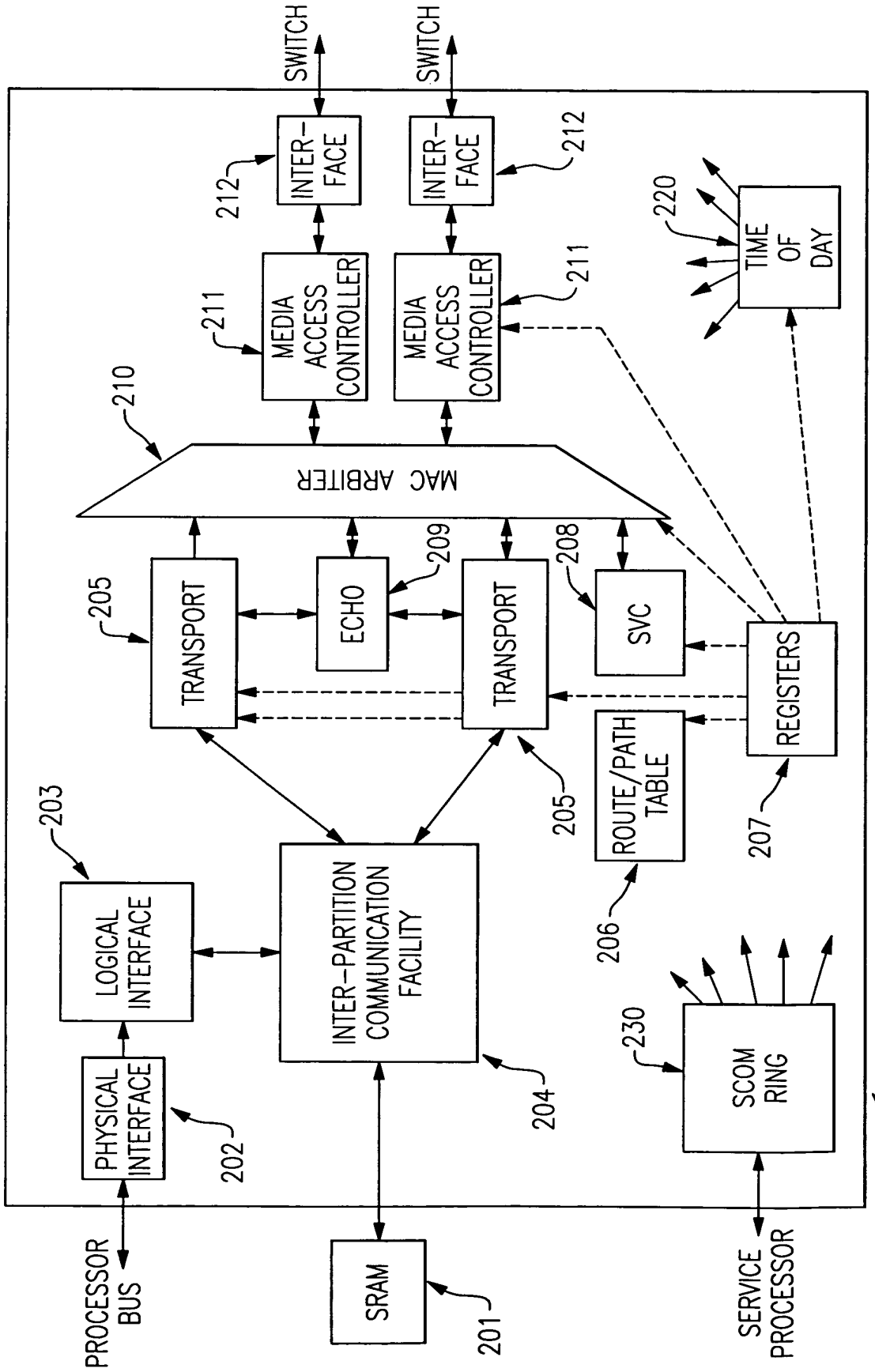
SWITCH
SWITCH
INTER-FACE
INTER-FACE
212
212
MEDIA ACCESS CONTROLLER
MEDIA ACCESS CONTROLLER
211
211
TIME OF DAY
220
210
MAC ARBITER
TRANSPORT
ECHO
TRANSPORT
SVC
205
209
208
REGISTERS
ROUTE/PATH TABLE
205
207
206
203
LOGICAL INTERFACE
INTER-PARTITION COMMUNICATION FACILITY
204
SCOM RING
230
PHYSICAL INTERFACE
202
200
PROCESSOR BUS
SRAM
201
SERVICE PROCESSOR

FIG.38

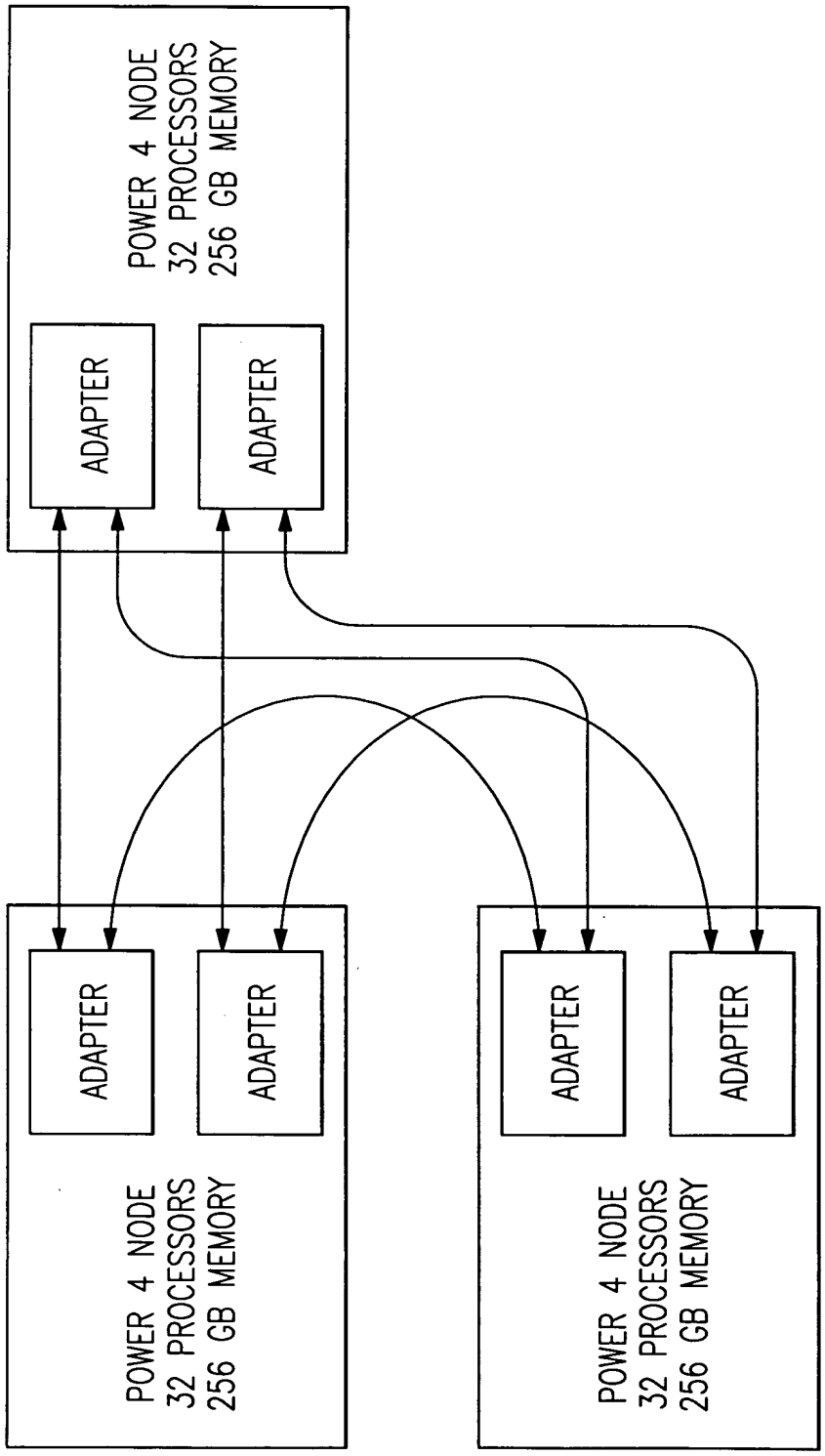
POWER 4 NODE
32 PROCESSORS
256 GB MEMORY
ADAPTER
ADAPTER
ADAPTER
ADAPTER
POWER 4 NODE
32 PROCESSORS
256 GB MEMORY
ADAPTER
ADAPTER
POWER 4 NODE
32 PROCESSORS
256 GB MEMORY

FIG.39

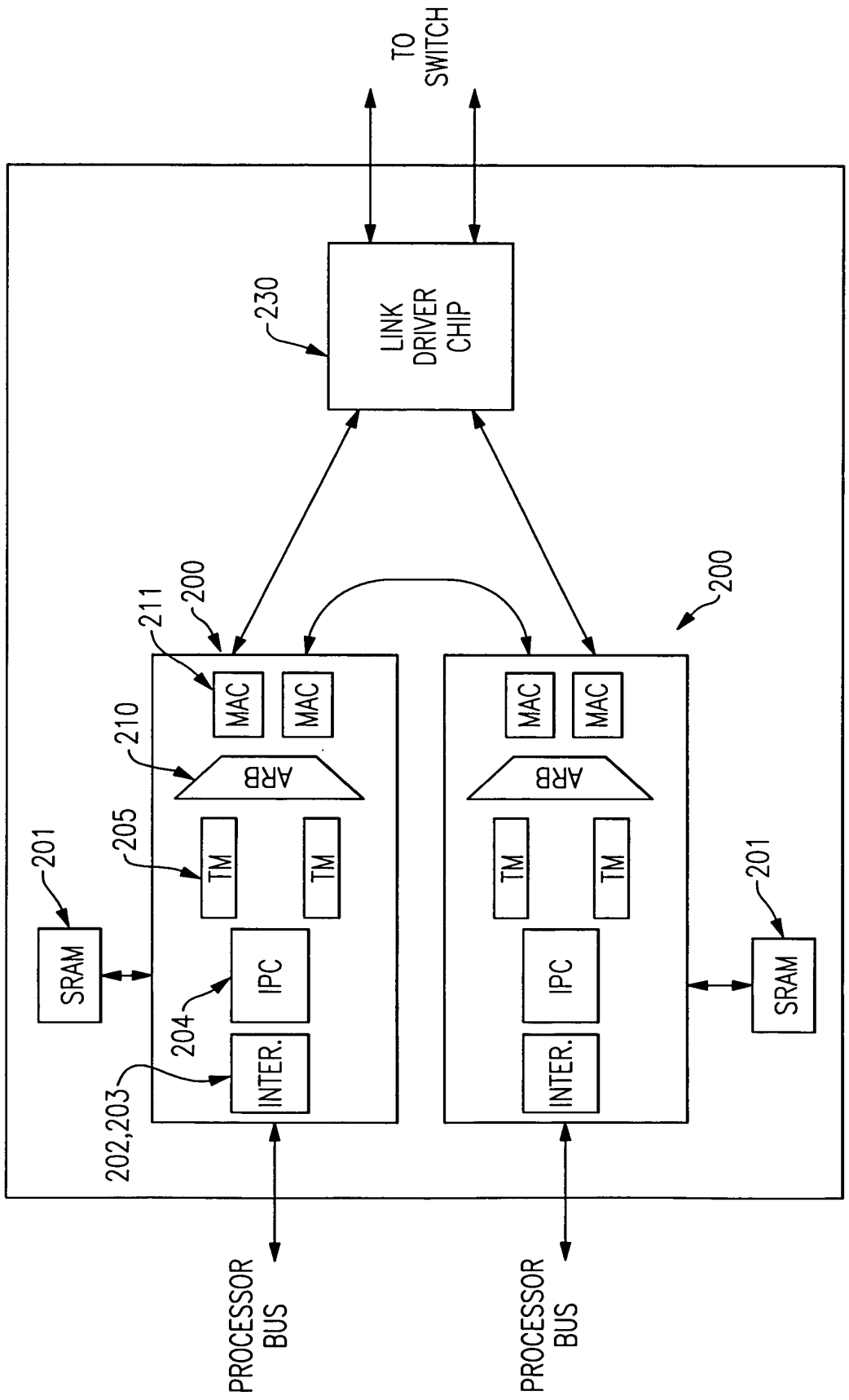
TO SWITCH
230
LINK DRIVER CHIP
200
211
MAC
MAC
210
ARB
205
TM
TM
201
SRAM
IPC
204
INTER.
202,203
PROCESSOR BUS
200
MAC
MAC
ARB
TM
TM
IPC
INTER.
201
SRAM
PROCESSOR BUS

FIG.40

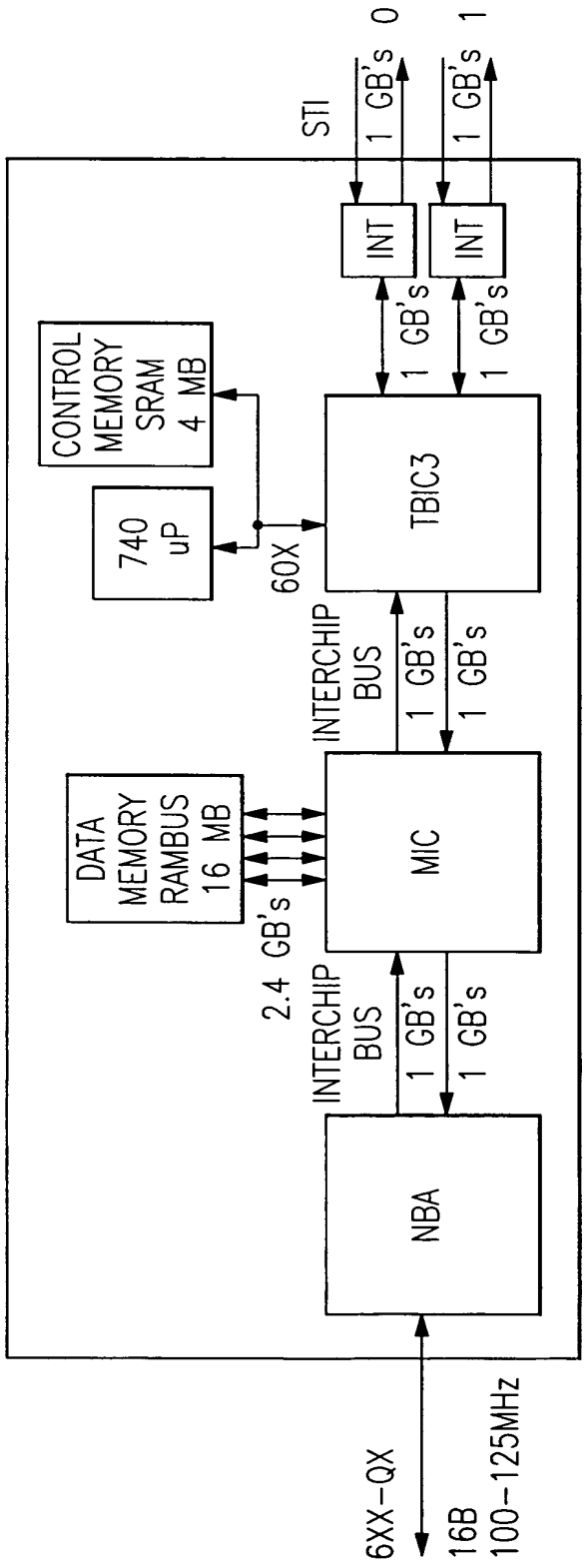
STI
1 GB's 0
1 GB's 1
INT
INT
1 GB's
1 GB's
CONTROL MEMORY SRAM 4 MB
740 uP
60X
TBIC3
INTERCHIP BUS
1 GB's
1 GB's
DATA MEMORY RAMBUS 16 MB
2.4 GB's
MIC
INTERCHIP BUS
1 GB's
1 GB's
NBA
6XX-QX
16B
100-125MHz

FIG.41

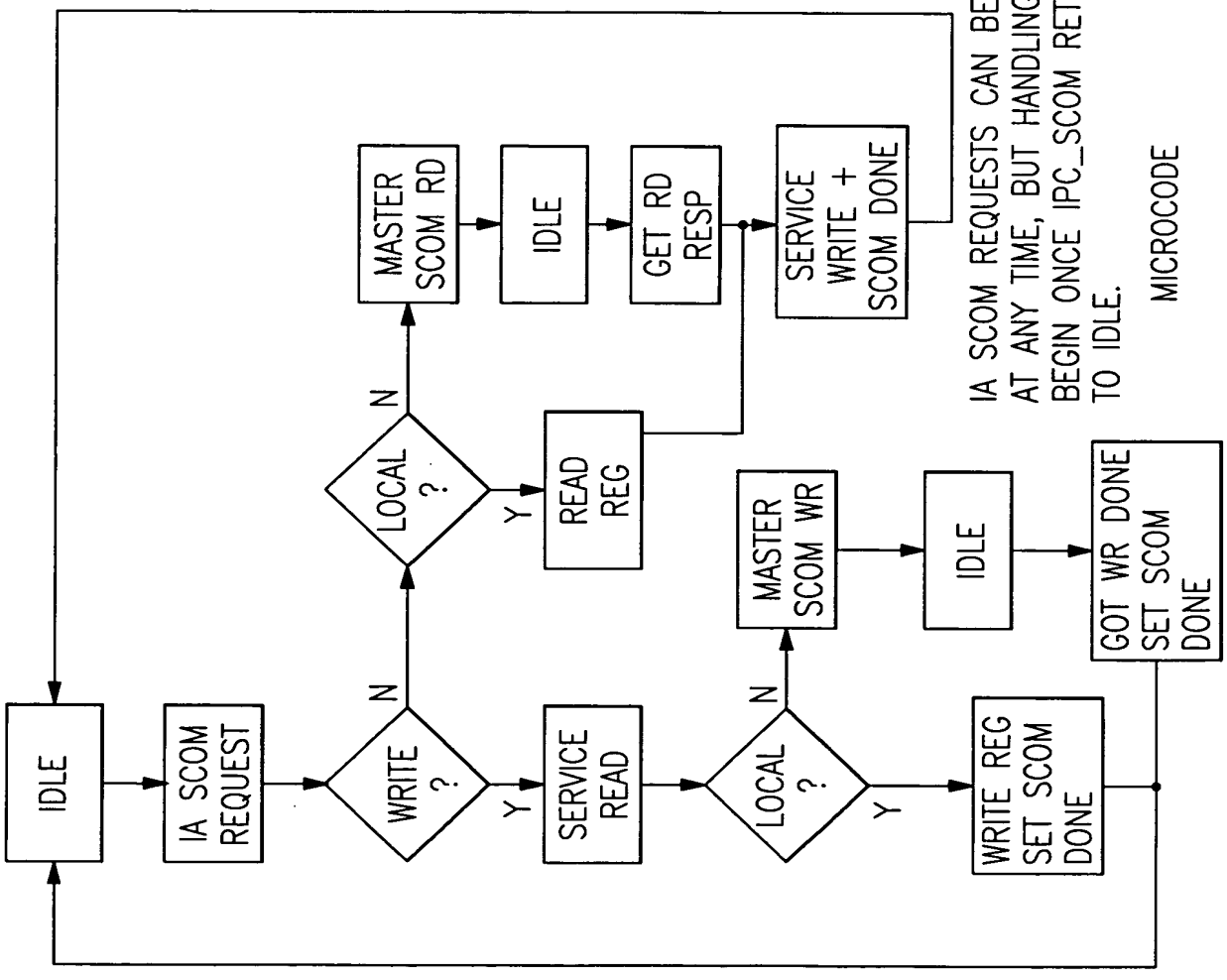
IDLE
IA SCOM REQUEST
WRITE ?
N
Y
SERVICE READ
LOCAL ?
N
Y
WRITE REG SET SCOM DONE
MASTER SCOM WR
IDLE
GOT WR DONE SET SCOM DONE
LOCAL ?
N
Y
READ REG
MASTER SCOM RD
IDLE
GET RD RESP
SERVICE WRITE + SCOM DONE
IA SCOM REQUESTS CAN BE CAPTURED AT ANY TIME, BUT HANDLING WILL ONLY BEGIN ONCE IPC_SCOM RETURNS TO IDLE.
MICROCODE

FIG.42

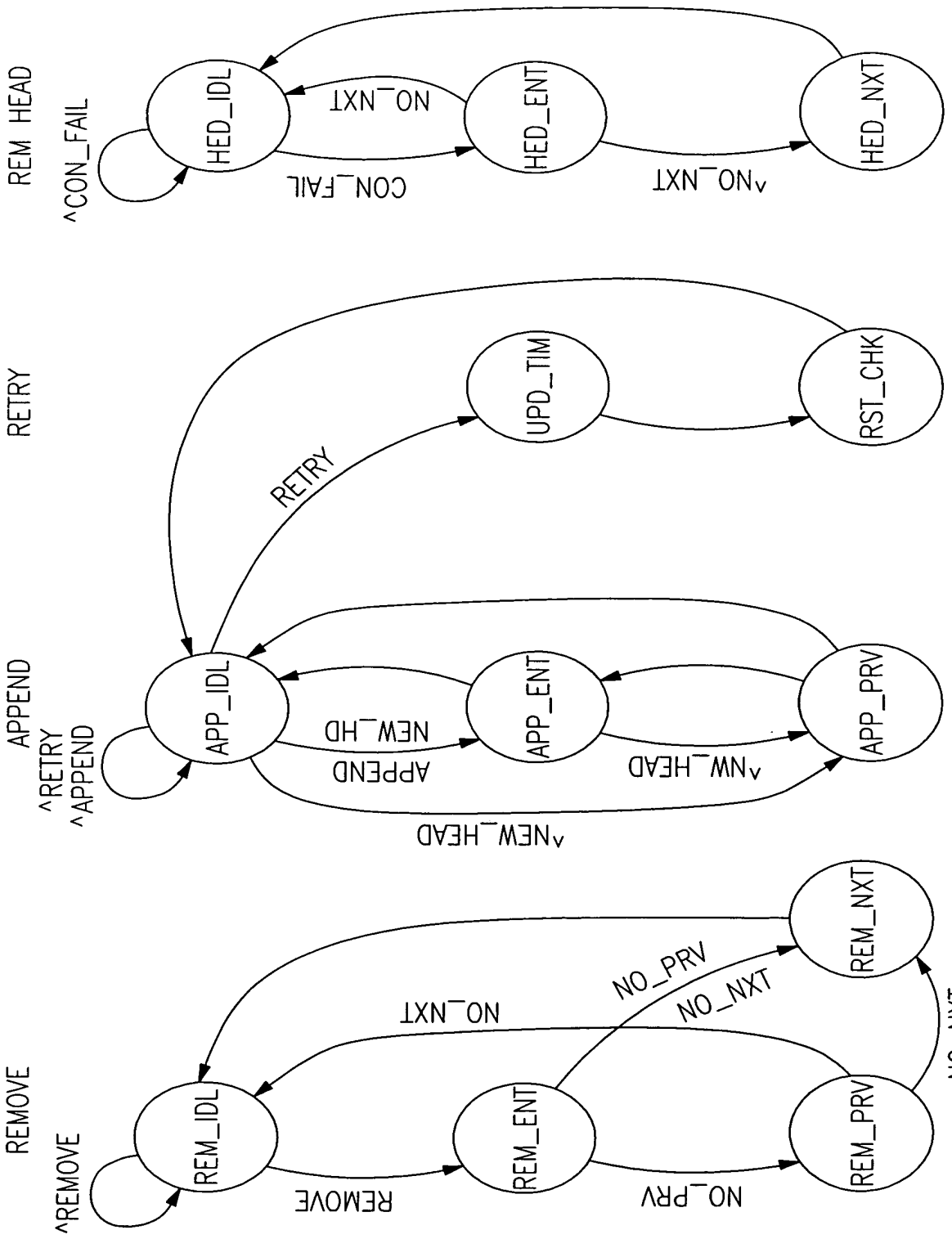
REM HEAD
^CON_FAIL
HED_IDL
NO_NXT
CON_FAIL
HED_ENT
^NO_NXT
HED_NXT
RETRY
UPD_TIM
RST_CHK
RETRY
APPEND
^RETRY
^APPEND
APP_IDL
NEW_HD
APPEND
APP_ENT
^NW_HEAD
APP_PRV
^NEW_HEAD
REMOVE
^REMOVE
REM_IDL
NO_NXT
NO_PRV
NO_NXT
REM_NXT
REMOVE
REM_ENT
NO_PRV
REM_PRV
NO_NXT

FIG.43

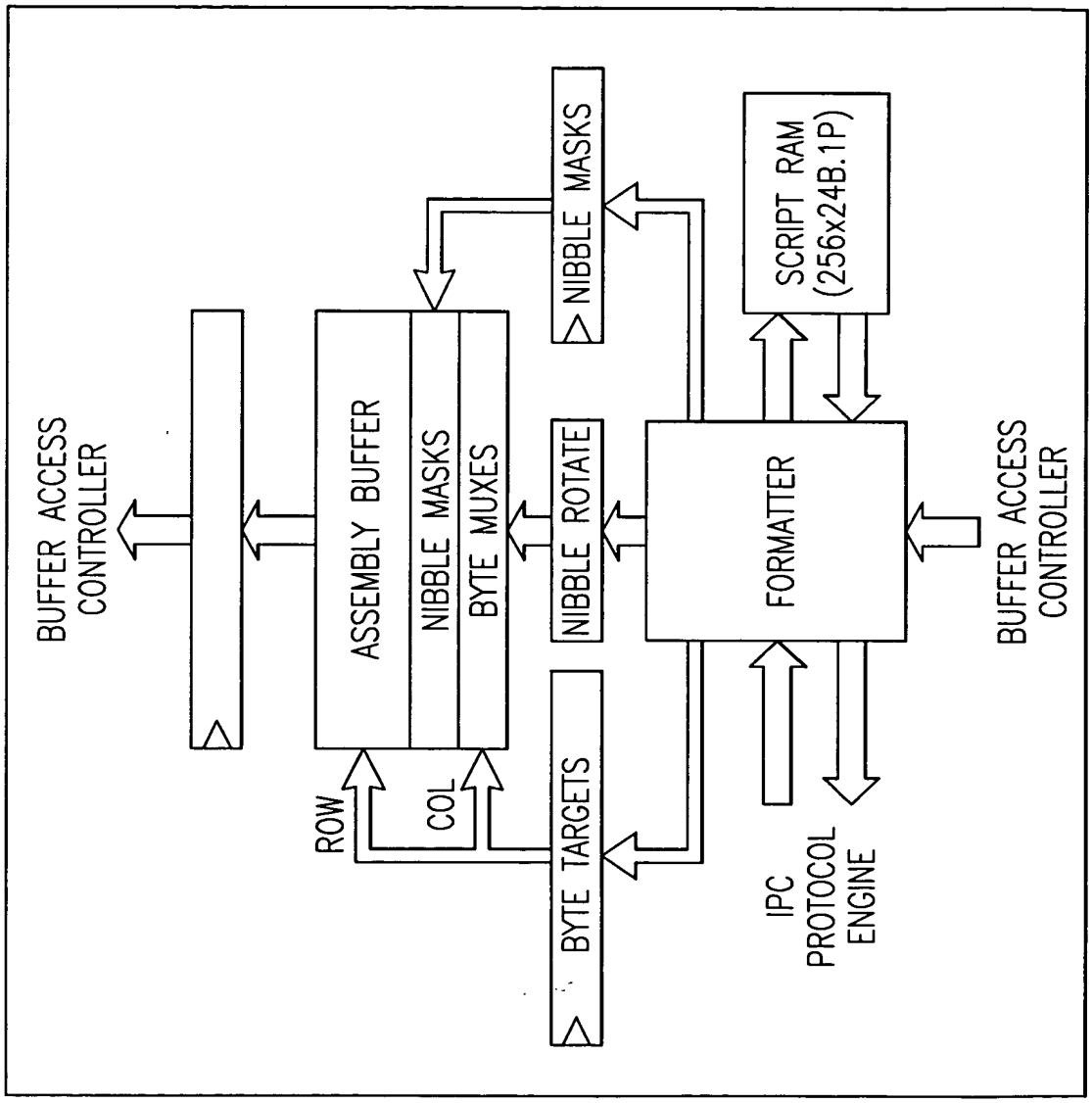
BUFFER ACCESS CONTROLLER
ASSEMBLY BUFFER
NIBBLE MASKS
BYTE MUXES
NIBBLE MASKS
SCRIPT RAM (256x24B.1P)
NIBBLE ROTATE
FORMATTER
BUFFER ACCESS CONTROLLER
ROW
COL
BYTE TARGETS
IPC PROTOCOL ENGINE

FIG.44

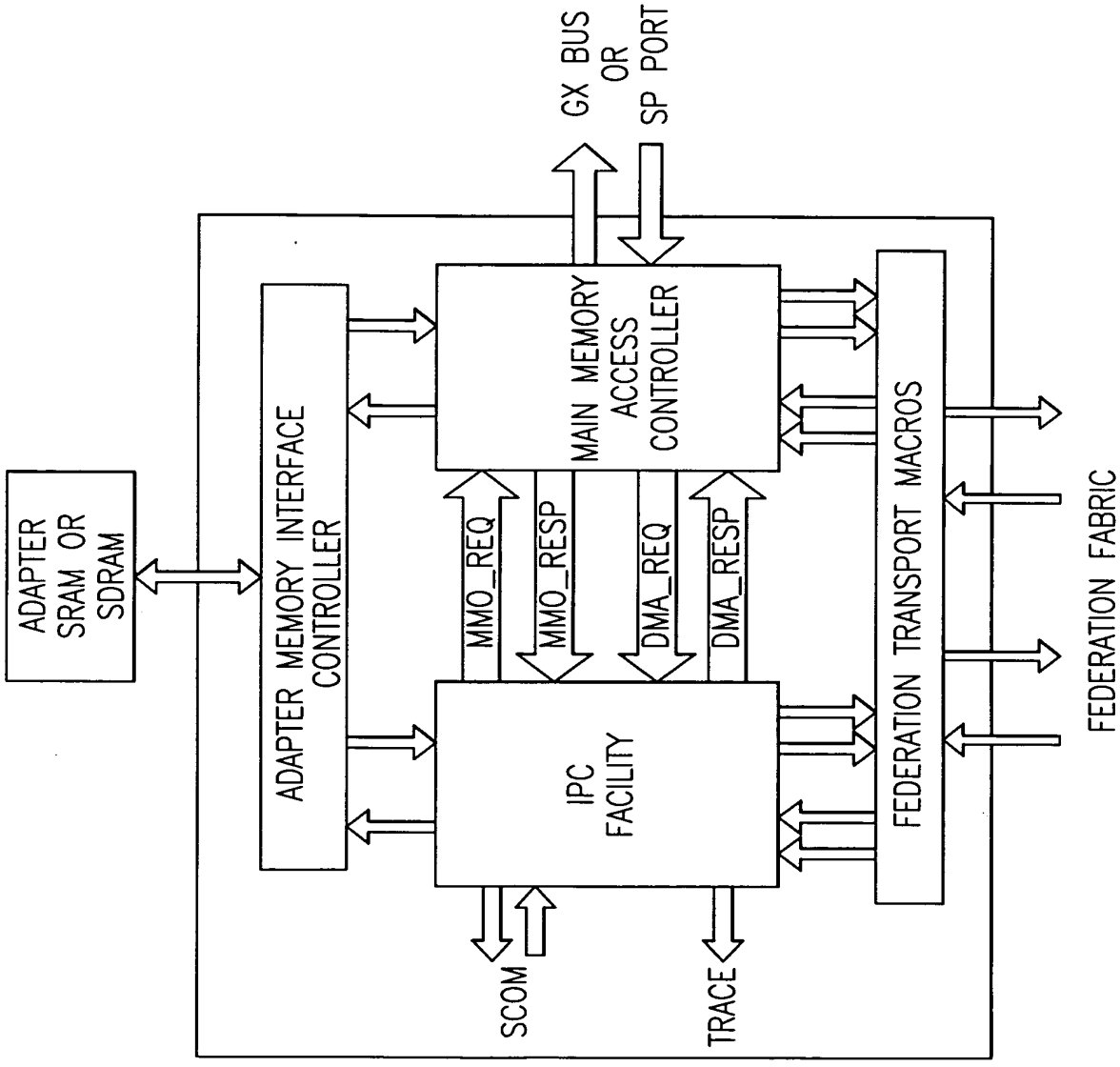
GX BUS OR SP PORT
ADAPTER SRAM OR SDRAM
ADAPTER MEMORY INTERFACE CONTROLLER
MAIN MEMORY ACCESS CONTROLLER
MMO_REQ
MMO_RESP
DMA_REQ
DMA_RESP
IPC FACILITY
FEDERATION TRANSPORT MACROS
FEDERATION FABRIC
SCOM
TRACE

FIG.45

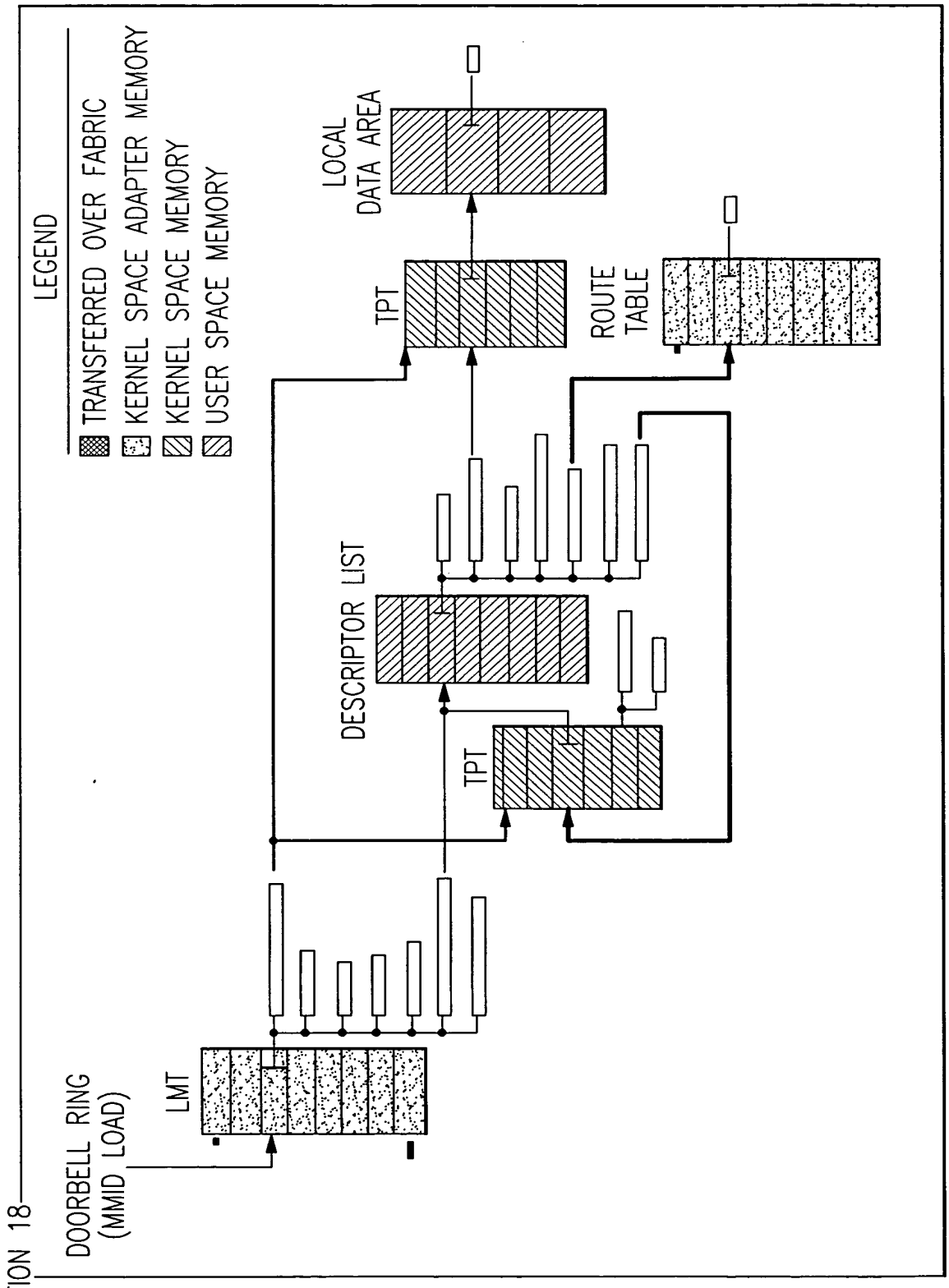
SECTION 18
DOORBELL RING
(MMID LOAD)
LMT
LEGEND
TRANSFERRED OVER FABRIC
KERNEL SPACE ADAPTER MEMORY
KERNEL SPACE MEMORY
USER SPACE MEMORY
LOCAL
DATA AREA
TPT
ROUTE
TABLE
DESCRIPTOR LIST
TPT

FIG.46

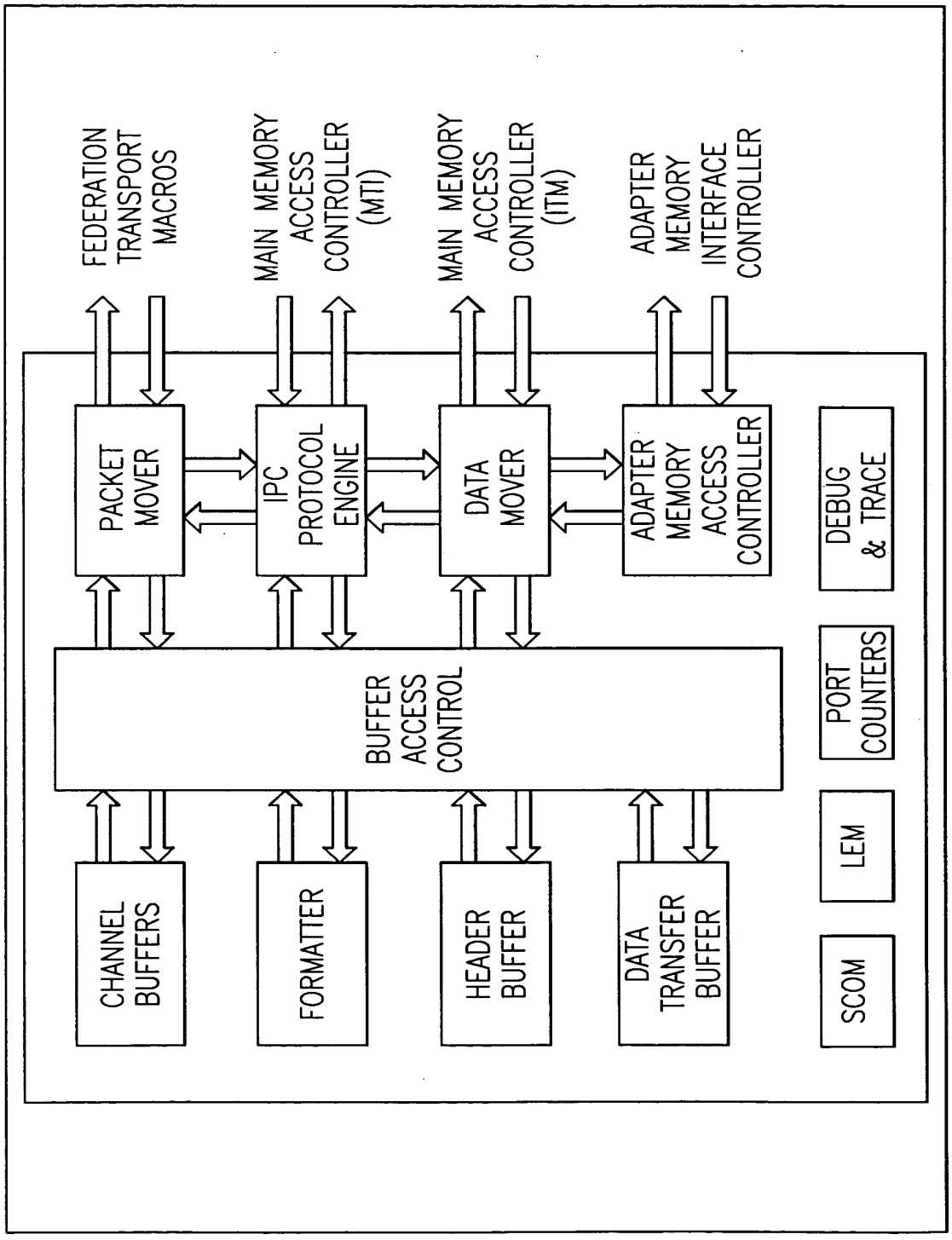
FEDERATION TRANSPORT MACROS
MAIN MEMORY ACCESS CONTROLLER (MTI)
MAIN MEMORY ACCESS CONTROLLER (ITM)
ADAPTER MEMORY INTERFACE CONTROLLER
PACKET MOVER
IPC PROTOCOL ENGINE
DATA MOVER
ADAPTER MEMORY ACCESS CONTROLLER
DEBUG & TRACE
BUFFER ACCESS CONTROL
PORT COUNTERS
LEM
SCOM
CHANNEL BUFFERS
FORMATTER
HEADER BUFFER
DATA TRANSFER BUFFER

FIG.47

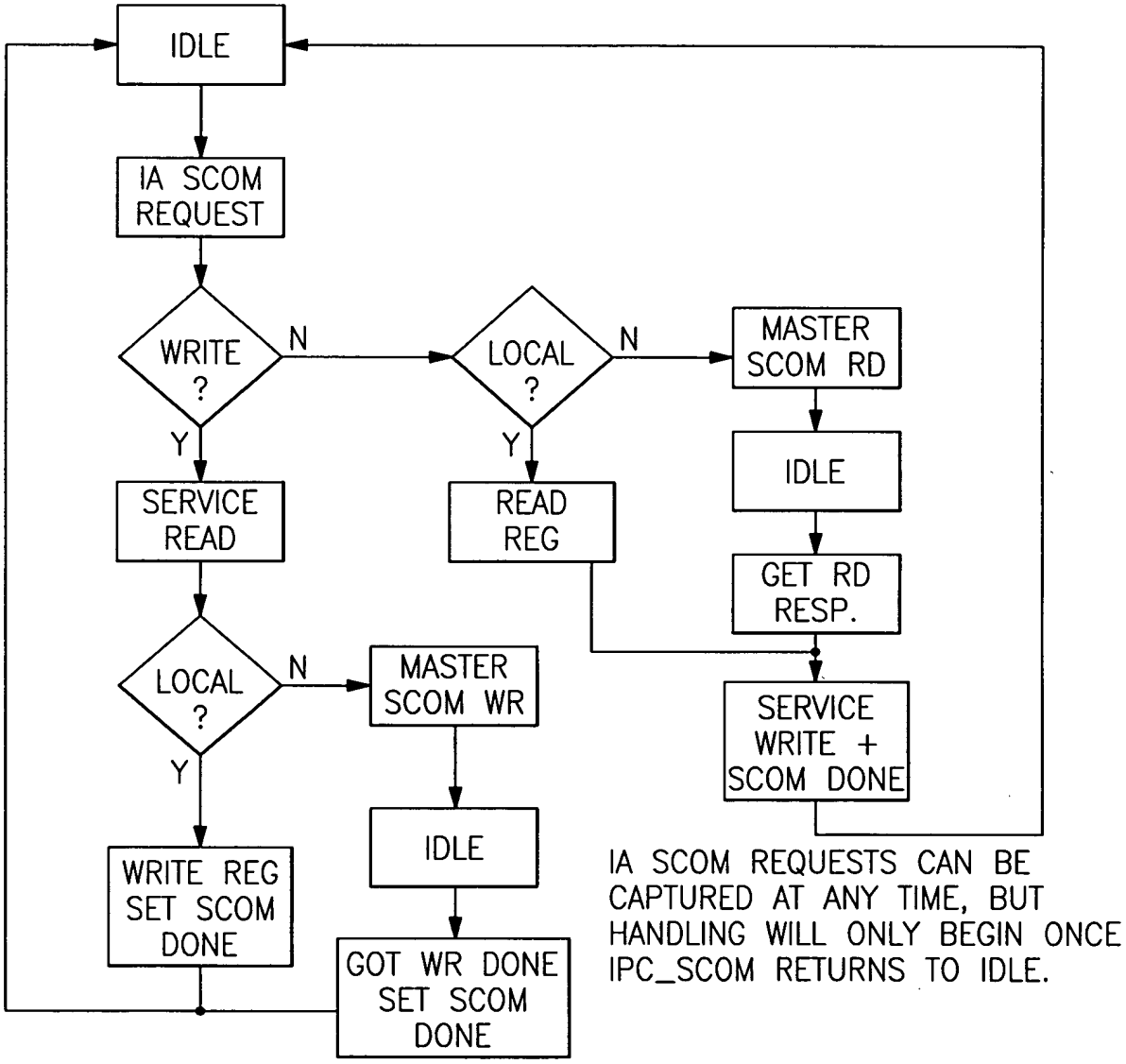
IDLE
IA SCOM REQUEST
WRITE ?
N
Y
LOCAL ?
N
Y
MASTER SCOM RD
IDLE
GET RD RESP.
SERVICE READ
READ REG
LOCAL ?
N
Y
MASTER SCOM WR
IDLE
SERVICE WRITE + SCOM DONE
WRITE REG SET SCOM DONE
GOT WR DONE SET SCOM DONE
IA SCOM REQUESTS CAN BE CAPTURED AT ANY TIME, BUT HANDLING WILL ONLY BEGIN ONCE IPC_SCOM RETURNS TO IDLE.

FIG.48

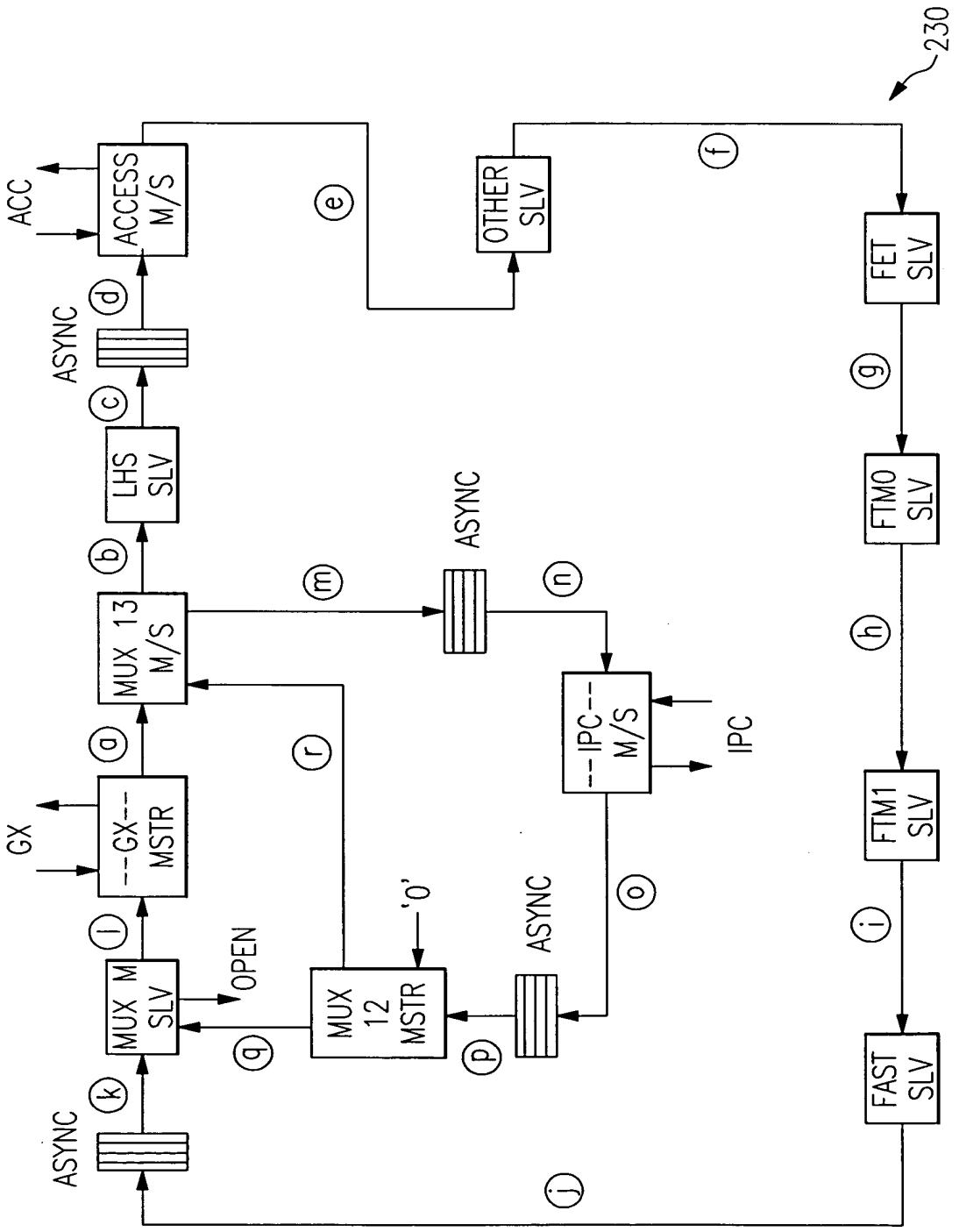
230
ACC
ACCESS M/S
ASYNC
LHS SLV
MUX 13 M/S
GX
--GX-- MSTR
MUX M SLV
OPEN
ASYNC
MUX 12 MSTR
'0'
ASYNC
--IPC-- M/S
IPC
OTHER SLV
FET SLV
FTM0 SLV
FTM1 SLV
FAST SLV
a
b
c
d
e
f
g
h
i
j
k
l
m
n
o
p
q
r

FIG.49

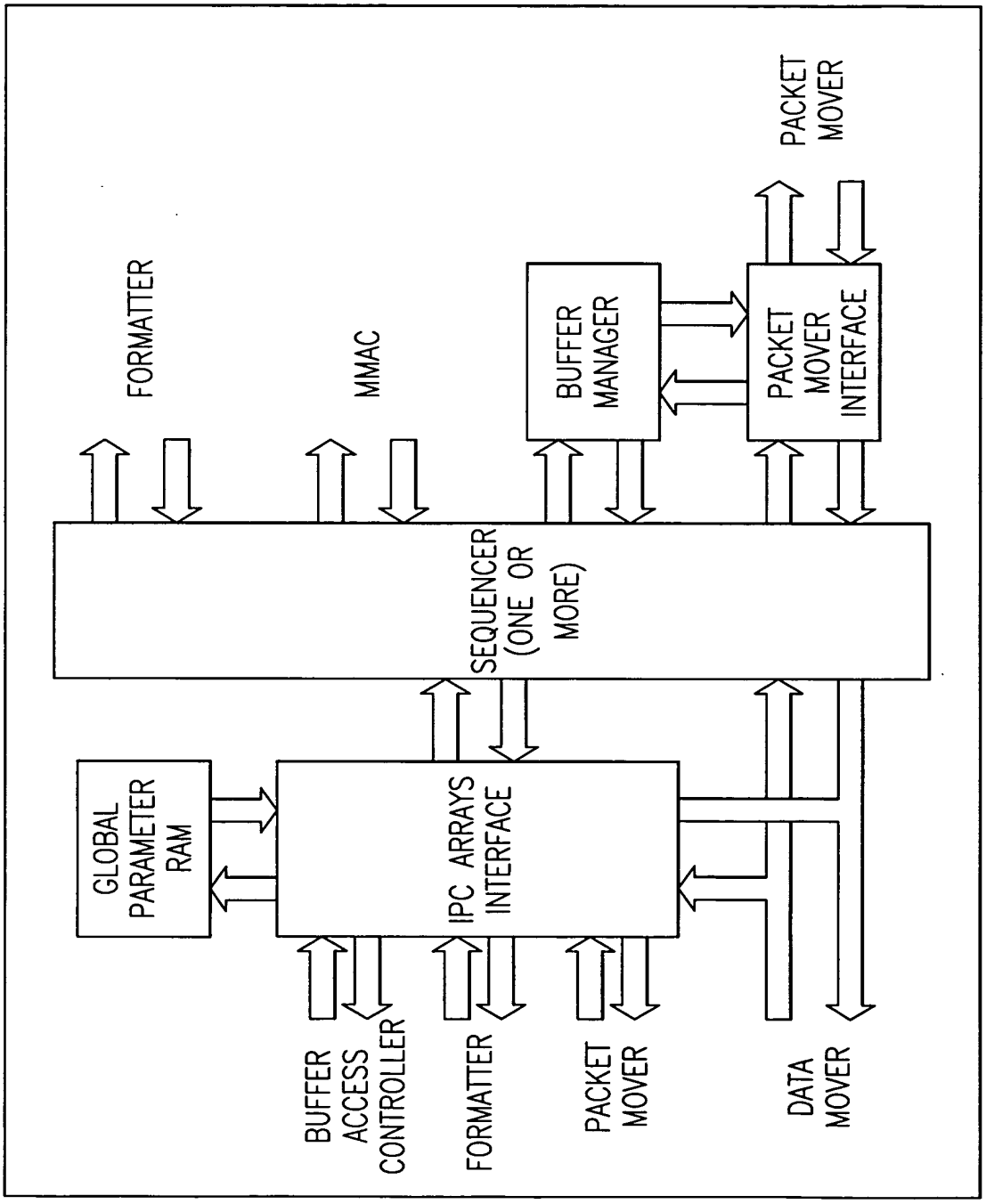
PACKET MOVER
FORMATTER
MMAC
BUFFER MANAGER
PACKET MOVER INTERFACE
SEQUENCER (ONE OR MORE)
GLOBAL PARAMETER RAM
IPC ARRAYS INTERFACE
BUFFER ACCESS CONTROLLER
FORMATTER
PACKET MOVER
DATA MOVER

FIG.50